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THIRTY-FOUR MEGABIT FOUR-CHANNEL MULTIPLEXER

By

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OCTOBER 1985

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This technical report has been reviewed and is approved for publication.

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A four-channel high speed multiplexer/rate converter has been designed to permit the Digital European Backbone (DEB) system to utilize Conference of European Post and Telecommunications Administration (CEPT) Level 3 transmission facilities. The multiplexer combines two mission bit stream data channels each at 12.928 Mb/s, a data channel at 2.048 Mb/s, and a service channel bit stream at 192 kb/s into a composite data stream at 34.368 Mb/s. All data clocks can be asynchronous, since "bit stuffing" is employed. A demultiplexer that performs the inverse function is part of the full-duplex system.

A design approach that easily adspts to other data rates and frame formats is used. This report describes the theory snd operation of the prototype equipment.

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SECTION 1

INTRODUCTION

1.1 BACKGROUND

The Digital European Backbone (DEB) project is in the process of upgrading the transmission facilities of the Defense Communications System (DCS) in Europe. The system is evolving from frequency division multiplex (FDM) to time division multiplex (TDM) equipment. The bulk of the new transmission facilities consists of line-of-sight (LOS) radio links. These radio links will use Digital Radio and Multiplex Acquisition (DRAMA) TDM equipment.

In some instances the DCS will interconnect with host nation and NATO facilities. Interconnection and interoperability present problems because of incompatible digital data rates, formats, and equipment sets. At the Supreme Headquarters Allied Powers Europe (SHAPE) facility in Belgium, there is a requirement to transmit a DEB mission bit stream (MBS), whose data rate is 12.928 megabits per second (Mb/s), and a service channel bit stream (SCBS), whose data rate is 192 kilobits per second (kb/s), via fiber optic and coaxial cables. The SHAPE Command Center has multiple fiber optic connection entry points using a diverse routing configuration. The fiber optic cables are laid underground with access at underground repeater and reconstitution nodes. Initially, NATO was to operate and logistically support these repeaters operating at the Conference of European Post and Telecommunications (CEPT) Level 3 rate of 34.368 Mb/s.

1.2 CANDIDATE SOLUTIONS

Given the constraint that the fiber optic repeaters are to operate at 34.368 Mb/s using CEPT Level 3 equipment, there are two candidate solutions to the DEB/SHAPE interconnect problem. One solution depends on a special piece of interconnect equipment called the Digital Channel Efficiency Model (DCEM), being developed by the Digital Communications Corporation (DCC) under the sponsorship of the Rome Air Development Center (RADC). One of the modes of operation of the DCEM is as a rate converter between a DEB digroup rate of 1.544 Mb/s and a CEPT Level 1 (NATO) rate of 2.048 Mb/s. In accordance with the DRAMA/DEB multiplex hierarchy, the MBS can be demultiplexed into its eight constituent channels, each at 1.544 Mb/s. A set of eight DCEMs can be used to convert these 1.544-Mb/s signals to eight 2.048-Mb/s signals. Once in the NATO/CEPT multiplex hierarchy of digital group rates, CEPT Level 2 equipment can convert four 2.048-Mb/s data channels to a European

8.448-Mb/s data stream. Similarly, four 8.448-Mb/s data streams can be multiplexed into a CEPT Level 3 data stream of 34.368 Mb/s. The digroup rate conversion design structure is shown in figure 1. The problem of accommodating the 192-kb/s service channel bit stream remains. In the DCEM-based configuration (figure 1) the service channel would have to utilize separate dedicated coaxial cables for clock and data or be put onto mission channels by further breaking down one of the digroups to its constituent 24 channels, 3 of which would provide the capacity of the SCBS.

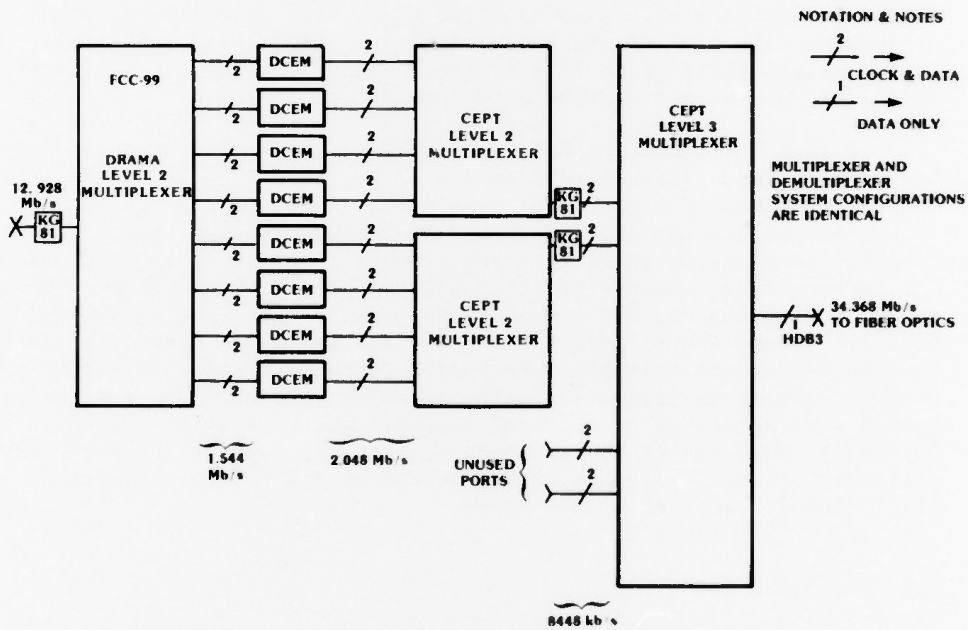


Figure 1. DRAMA/DEB-CEPT Level 3 Interconnect Using Digital Channel Efficiency Model

An alternative solution is to build a multiplexer that combines the MBS and SCBS into a single composite bit stream at the CEPT Level 3 rate. Because of the available channel capacity, two mission bit streams (MBS), a service channel bit stream (SCBS), and a 2.048-Mb/s (CEPT Level 1) data channel can easily be multiplexed up to the CEPT Level 3 rate. The configuration using the proposed multiplexer for the DEB/SHAPE interconnect is shown in figure 2.

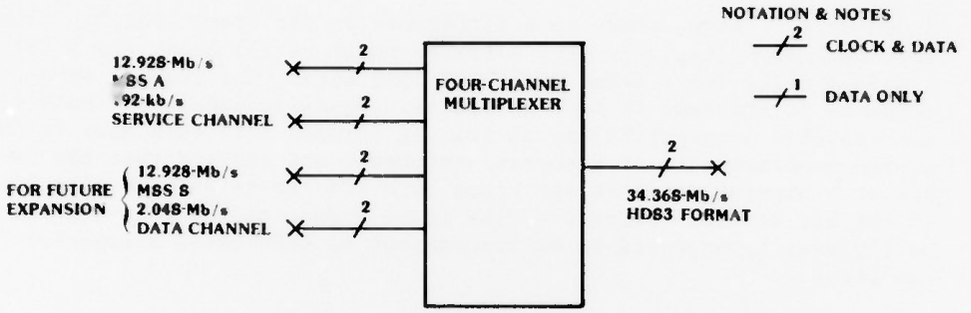


Figure 2. DRAMA/DEB-CEPT Level 3 Interconnect Using Four-Channel Multiplexer

A comparison of figures 1 and 2 shows that the four-channel multiplexer provides a great economy of equipment. It also saves a considerable amount of power and rack space. The four-channel multiplexer permits expansion by providing the spare MBS and 2.048-Mb/s data channels, and will do so with no additional cost in hardware, power, or system complexity. For those reasons the four-channel multiplexer is the preferred technical approach for the interconnection of DEB and NATO facilities, under the constraint of using CEPT Level 3 repeaters.

1.3 SYSTEM DESIGN CONSIDERATIONS

The DEB system is presently asynchronous and independent of NATO and European telephone systems. (However, a timing and synchronization system will be deployed at DCS stations in the late 1980s.) This independence has forced the design of the four-channel multiplexer to support four asynchronous data rates. Also, the proposed use of the high speed four-channel multiplexer, in conjunction with a fiber optic link that is extremely stable with respect to transmission errors, makes the loss of framing and pulse stuff information that could lead to loss of bit count integrity (BCI) very unlikely. Therefore, a virtually error-free transmission medium allows the use of asynchronous operation, which in turn facilitates an easier system timing interface.

The standards for the CEPT Level 3 data rate are described in section G.751 of the CCITT standards. The four-channel multiplexer cannot strictly comply with the entire standard because it is multiplexing data streams other than CEPT Level 2 (whose rate is

8.448 Mb/s). Also, there is a difference in the frame lengths. The four-channel multiplexer uses a frame length of 256 bits; the G.751 standard calls for a frame length of 1536 bits. The framing word sequence is the same in both instances. Specific inquiries concerning the possible incompatibility of framing formats have been made to one of the manufacturers of European equipment, who replied that the repeater equipment monitors the frame bits for errors with no alteration of the bit stream. Therefore, the frame format of the four-channel multiplexer is expected to be transparent to CEPT Level 3 repeater equipment.

SECTION 2

DESIGN DEFINITION

The 34-Mb/s, four-channel multiplexer was designed for the purpose of permitting DEB DRAMA data rates to be transmitted over European equipment using CEPT Level 3 standards. The multiplexer combines four data streams, two at 12.928 Mb/s, one at 2.048 Mb/s, and one at 192 kb/s, into a composite data stream of 34.368 Mb/s. The demultiplexer portion of the system performs the inverse operation of separating out the four channels from the 34-Mb/s data stream. The 34-Mb/s data stream uses HDB3 coding, as described in CCITT standard G.703, and uses a framing header, as described in standard G.751.

The 12.928-Mb/s data rates are the MBS rates carried by the AN/FRC-17X (X = 0, 1, 2, 3) series of radios, as generated by the AN/FCC-99 multiplexer, in the DRAMA equipment family. DRAMA radios use the 192-kb/s service channel bit stream data rate. A service channel bit stream can come from a three-channel version of an AN/FCC-98 multiplexer or from an AN/FCC-100 (low speed, time division) multiplexer. The 2.048-Mb/s rate corresponds to the CEPT Level 1 digroup data rate, which was added to the multiplexer design at the request of SHAPE.

The multiplexer operates with asynchronous bit streams, using positive bit stuffing for each data rate. The long term destuff jitter on the demultiplexer side is less than 50 nanoseconds (ns) for each data rate.

The multiplexer, demultiplexer, and power supplies are packaged in a single cabinet, which comprises one terminal end of a full-duplex system. Two multiplexer equipment cabinets and a switchover chassis can be connected to form a fully redundant four-channel multiplexer, with automatic switchover, giving protection in case of failure of one of the units. The simplest site maintenance concept would be the replacement of an entire four-channel multiplexer unit.

The major subchassis of each cabinet are the power supply chassis and card cage. The power supply chassis consists of individual power supplies providing the various voltages used by the system. The card cage contains the wire wrap boards. The boards, either TTL or ECL, are designed to contain functional circuits that require a minimum of interconnect.

The four-channel multiplexer contains a limited amount of built-in test equipment (BITE). The BITE monitors the power supplies and activity at key locations for each of the data rates at both the multiplexer and demultiplexer. Demultiplexer frame acquisition is also monitored. Although the BITE circuitry does not find faults down to the individual board level, it is an efficient warning indicator and troubleshooting aid.

SECTION 3

FRAME STRUCTURE

3.1 BIT STUFFING

The composite data stream at the 34.368-Mb/s data rate contains all the data in each of the input data streams, as well as some overhead data, packed in a well defined manner, called the frame structure. The sum of the input data rates is less than the output (34.368-Mb/s) data rate. Since the input data streams are asynchronous with respect to the 34.368-Mb/s output rate, the frame structure must accommodate some small amount of variability in the number of bits per input data stream per frame. This accommodation of slightly variable data rates is called bit stuffing.

3.2 FRAME USAGE

The frame structure of the four-channel multiplexer is shown in appendix A. There are 256 bits in a frame. The first 10 bits (1111010000) are the framing bits, which designate the beginning of the frame. In CCITT Standard G.751, the 11th bit is reserved for remote fault status; the 12th bit is reserved for national use. To avoid incompatibility with CEPT Level 3 transmission equipment, those 2 bits are not specified. The bits corresponding to each input data stream, as well stuff control bits, are nearly evenly distributed throughout the remainder of the frame. All data rates, including the output data rate, are divisible by 64,000, as shown below:

$$\frac{34.368 \times 10^6}{64 \times 10^3} = 537$$

$$\frac{12.928 \times 10^6}{64 \times 10^3} = 202$$

$$\frac{2.084 \times 10^6}{64 \times 10^3} = 32$$

$$\frac{192 \times 10^3}{64 \times 10^3} = 3$$

Using the factors derived above, one can compute the average number of data bits per frame for each data rate using the following:

a. Average number of bits per 256-bit frame for each of the 12.928-Mb/s channels:

$$\frac{202 \times 256}{537} = 96.3$$

b. Average number of bits per frame for the 2.048-Mb/s rate:

$$\frac{32 \times 256}{537} = 15.3$$

c. Average number of bits per frame for the 192-kb/s rate:

$$\frac{3 \times 256}{537} = 1.43$$

Because each frame can include only an integer number of bits for each data rate, the MBS rate (of 12.928 Mb/s) must be accommodated by 96 bits in some frames and 97 bits in others. Therefore, in certain frames (approximately 30 percent), undesignated because of the asynchronous nature of this design, a 97th data bit must be added. In other frames this bit is stuffed (and subsequently discarded at the demultiplex end). Similar reasoning is used for each of the other data rates (15 bits plus 1 stuff bit for the 2.048-Mb/s channel; 1 bit plus 1 stuff bit for the 192-kb/s channel). The frame structure must also have a means of signaling the remote demultiplexer to confirm whether or not the stuff position contains valid data. For each of the four data streams in the frame, there is a stuff control word consisting of 3 bits at predetermined locations. This provides a measure of noise immunity by allowing a majority vote to determine the status of the stuff bit.

The frame usage is shown below:

Data Type	Frame Bit Usage
MBS A (12.928 Mb/s)	96 data bits 1 stuff bit 3 stuff control bits
MBS B (12.928 Mb/s)	96 data bits 1 stuff bit 3 stuff control bits
CEPT level 1 (2048 kb/s)	15 data bits 1 stuff bit 3 stuff control bits
SCBS (192 kb/s)	1 data bit 1 stuff bit 3 stuff control bits
Framing and status	12
Undesignated	20
Total	256

SECTION 4

BLOCK DIAGRAM AND OPERATION

4.1 TRANSMIT SIDE

Figure 3 shows the block diagram of the multiplexer/demultiplexer. For each data channel, there is an elastic storage memory: first-in first-out (FIFO) buffer. The FIFO permits a data load clock and a data unload clock to operate asynchronously with each other. Data bits are unloaded from the memory in the same order as they were originally loaded into the memory. For error-free operation, the average output data rate must equal the input data rate. Also, the absolute difference in bit count between the input and output clock counts cannot exceed the memory size. On the FIFO usage, there are other constraints that are related to device characteristics and circuit details.

Each data source, such as an AN/FCC-99 (12.928 Mb/s) or AN/FCC-98 (192 kb/s), clocks data into its respective FIFO in the multiplexer. Data are unloaded from each FIFO in accordance with the frame format, such that the average output data rate equals the input data rate. The decision to unload or not to unload data from any FIFO at its stuff position time depends on the occupancy status of that FIFO at a certain time during the frame: In particular, if a FIFO is more than half full when the frame count reaches 128, then a data bit is unloaded into the channel's stuff position. If, however, the FIFO is less than half full, no data are unloaded at the stuff position time. Thus, the contents of each FIFO are regulated by use of the status bit. This regulation tends to keep each FIFO approximately half full.

A stuff control word is used to permit the receive end to distinguish between data/no data conditions. The stuff control word for each bit stream consists of 3 bits. All 3 bits are encoded high when the associated FIFO has an occupancy greater than half full, and are encoded low when the FIFO occupancy is less than half full. Three bits are used to prevent bit errors from causing destuff control errors due to noise in the transmission system. The data/stuff decisions at the receive side are based on majority votes on the 3 bits in each received stuff control word.

Data, framing, and control words are introduced into the data stream according to the frame format. A 34.368-MHz crystal controlled oscillator drives a modulo-256 binary counter. This counter

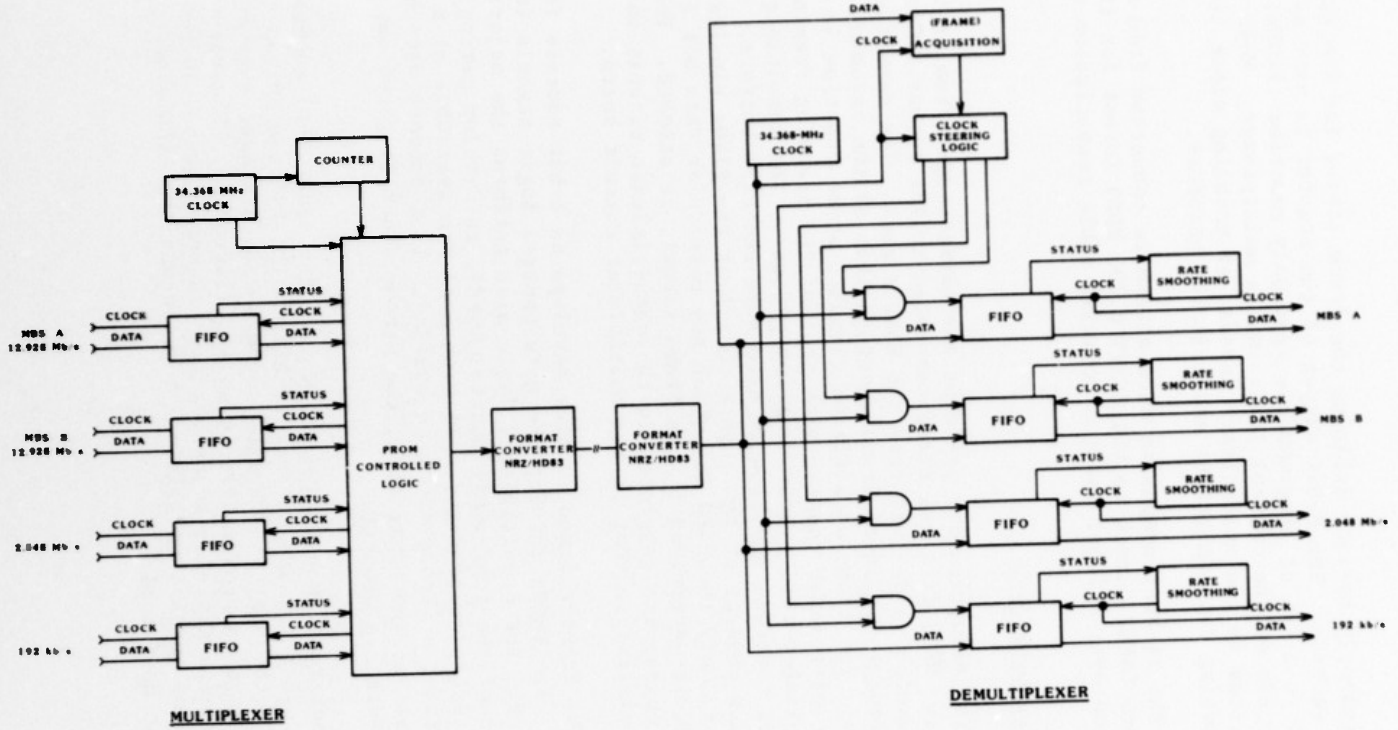


Figure 3. Block Diagram of Rate Converter

continuously cycles, defining the frame timing for the entire multiplex section. The 8-bit output of the counter is used as the address to a set of programmable read-only memories (PROMs) that are the basis of the control logic in the multiplexer. Most control functions in the multiplexer consist of enabling clock lines and addressing data selectors and priority encoders.

The 34-Mb/s composite data stream is converted from a nonreturn to zero (NRZ) format to the CCITT G.703 HDB3 format for transmission over a fiber optic or coaxial cable transmission system.

4.2 RECEIVE SIDE

The demultiplexer performs the inverse operation of the multiplexer. HDB3 data are first converted to NRZ format. Clocking information is derived from the HDB3 signal. The demultiplexer must synchronize its local frame count to that of the incoming bit stream. The frame acquisition circuit, whose function is to align the demultiplexer counter with that of the incoming framing word, accomplishes this synchronization process. The demultiplexer logic circuit controls the flow of data into the FIFO buffers. All data bits are present at the inputs to all of the FIFOs simultaneously; however, only the FIFO for which any particular data bit is intended, as determined by the frame format, is strobed. These strobe clock pulses are generated in the demultiplexer circuit in a manner quite similar to that of the multiplexer circuit board.

The frame-aligned counter develops an 8-bit address for some PROMs. The PROMs develop the gate control logic signals for clock steering. The demultiplexer logic also performs the majority vote on each of the four stuff control words, to develop gating signals at the pulse stuff times. If true data are available at a pulse stuff time, a strobe clock is enabled. If a correct data bit is not available at the stuff time, the strobe clock is gated out and the stuff data are dropped.

Each rate smoothing circuit (one for each FIFO) generates the unload clock for its respective FIFO. The average unload clock speed is the same as the load clock speed, averaged over an integration time of approximately 10 ms (milliseconds). The circuit operates by automatically adjusting the frequency of a VCXO (voltage controlled crystal oscillator) to maintain the FIFO's occupancy level at half full.

4.3 FAULT MONITORING

The multiplexer/demultiplexer has some built-in test equipment, to provide valuable monitoring assistance. The following parameters are monitored by the BITE logic.

a. Power supply voltage levels

b. Frame acquisition

c. Multiplexer FIFO half-full status activity

d. Demultiplexer FIFO half-full status activity

No attempt has been made to have the BITE isolate problems to the card level. However, the BITE monitors functional units to readily identify failures, if they should occur.

4.4 SYSTEM ADAPTATIONS

At each count in the frame, the multiplexer and the demultiplexer must perform well-defined operations. The essence of these operations is to steer clock pulses and data bits. Enabling lines, which control logic gates as a function of the frame count, perform these operations.

The control functions reside in high speed PROMs. A modulo-256 bit counter generates the address for the PROMs. The 34.368-Mb/s composite data rate clock drives these counters. Because of the unit's high speed operation (29-ns clocking interval), data are stored after each function, such as counting and data selection, to allow sufficient time for all digital operations to take place. In this "pipeline" configuration, critical race conditions are eliminated.

Those techniques permit the system to be easily modified to support other rates and frame structures. For example, a new frame structure could be calculated for a different data rate. Then a new set of PROMs could be programmed to reflect the changes. They would be the only changes required, except for the replacement of crystal oscillators in the rate smoothing circuits.

SECTION 5

CIRCUIT BOARD DESCRIPTIONS

5.1 CIRCUIT BOARD TYPES

The multiplexer and demultiplexer are divided into functional circuit boards. The circuit types required are listed below, along with quantity per unit and predominant logic family for each board type.

a. FIFO, 2, (TTL and analog)

b. Multiplexer, 1, (ECL)

c. HDB3 encoder, 1, (ECL)

d. HDB3 decoder, 1, (ECL)

e. Frame acquisition, 1, (ECL)

f. Demultiplexer, 1, (ECL)

g. BITE, 1, (TTL and analog)

h. Rate smoothing, 1, (TTL and analog)

The system was arranged into these types to minimize backplane wiring and simplify testing during the development phase. The interconnection between boards requires very few wires. The circuits are built on R-series wire-wrap boards, manufactured by Augat, Incorporated, of Attleboro, Massachusetts. Each card is approximately 7 inches square, with 60 integrated circuit (IC) positions for the TTL card and 60 IC positions for the ECL boards, of which 24 positions are reserved for translator gates. Few boards are densely populated. A single card cage accommodates both TTL and ECL boards. The cage has 13 slot positions, of which 9 are used by the 4-channel multiplexer. A separate position is reserved for a TTL test simulator board, which is not normally plugged in.

Since the output data rate of the four-channel multiplexer is 34.368 Mb/s, corresponding to a clock period of 29.1 ns, ECL is used for the high clock rate portions of the system. Except for voltage translation chips and analog circuitry, the cards are organized to be either all ECL or all TTL.

5.2 MULTIPLEXER BOARD

The multiplexer circuit board is designed to create the output frame format, based on instructions that are coded into the PROMs. The PROMs have 256 different addresses, which correspond to each of the bits in the frame format. (See appendix A.) The multiplex circuitry is used to control the generation of fixed frame bits, the selection of data from each of the four input FIFOs, the generation of FIFO unload clock pulses, and the setting of stuff control bits for asynchronous operation. Each bit in the 256-bit frame plays a defined role; the PROM is programmed to have the multiplexer insert the proper data or overhead bit into each of those locations. The only variables that affect multiplexer operation, other than the modulo-256 counter, are the FIFO status indicators, whose values determine whether or not stuffing will take place in a given frame for a given channel.

The multiplexer circuit schematic is shown in figure B-1 in appendix B. The system clock (53) is located on the board. It is a 34.368-megahertz (MHz) crystal controlled oscillator with an ECL logic output. The clock drives a pair of OR gates (41), with multiple outputs for clock distribution. Since the frame is 256 bits long, a modulo-256 bit counter (25 and 37) is used as the input address for the PROMs. The output of the counter is registered by D-edge registers (26 and 38). The 8-bit address is the input to three ECL (10149) PROMs (27, 51, and 39), each organized for an 8-bit address (256) and a 4-bit output. The truth tables for each PROM are in appendix C. D_1, D_2, and D_3 outputs of PROM (27) develop an address for the 10564 8:1 chip selector (30). The output of the chip selector will be one of eight inputs, depending on the 3-bit address selected. Only six of eight possible inputs are used. These six inputs correspond to each of the four data ports or corresponding FIFO status lines and hard-wired "1" and "0," which are used to create the frame bits. The input from each of the four data channels will be either data or the occupancy state of its respective FIFO. The output, D0, of the 10149 PROM (27) controls the steering of the FIFO status or data to the 8:1 multiplexer by means of a 2:1 multiplexer (31). The outputs of the PROMs are registered, to enable the circuit chips to have a full clock cycle (29.1 ns) for propagation delays. The delay time between address and stable data at the output of the 10149 PROM is specified to be 25 ns, worst case. This pipeline technique is used throughout the entire high speed section of the design.

Both the occupancy status and the data from each of the FIFOs are converted to ECL logic levels from TTL levels by means of the 10524 voltage translator chips (19) and (20). The ECL cards have an area reserved for translator chips, where both ECL voltages (0,

-5, -2) and TTL voltages (+5) are available to the chip. The occupancy status of the FIFOs is held in a register (32), clocked once per frame.

Besides selecting data according to frame format, the multiplexer must develop unload clocks for each FIFO. PROM (51) develops an address for a 10562 (54) "one of eight" priority encoder. The four outputs (Q_0, Q_1, Q_2, and Q_3) of the decoder correspond to enabling lines for each of the respective clock gates (21) for the four FIFOs. The clock enable lines are high only at the "true" data time. They are low during stuff control times and stuff opportunity times. PROM (39) generates an enabling signal for each FIFO only during the stuff opportunity times, to control gates in (44). The FIFO occupancy status also controls IC (44). The "true" data clock enable and the possible "stuff opportunity" clock enable are "wire ORed" before being translated to the TTL level by (21).

5.3 FIFO BOARD

The FIFO board consists of four independent circuits. There are two high speed FIFO circuits for the two MBSs and two low speed FIFO circuits for the SCBS and the 2048-bit stream. The circuits are assembled on a TTL wire-wrap board; all logic on the board is TTL. The heart of each of the buffer circuits is the 74S225, a 16 by 5 asynchronous FIFO memory chip. These chips require a 20-pin socket that is not available on the R-series wire-wrap board. An adapter socket is used with each 74S225. The adapter socket permits four conventional IC sockets to accept the 20-pin adapter socket.

5.3.1 High Speed Circuit

Two 74S225s are placed in tandem, to create a FIFO that is 5 bits wide and 32 bits deep. Besides gaining depth, this configuration permits the use of the Input Ready (IR) flag of the downstream FIFO to be used as a greater than or less than half-full indicator.

The FIFO chip is rated for a clock speed up to 10 MHz. This speed limitation requires that the 12.928-Mb/s data rates be processed by converting the serial data stream into a slower rate, parallel data stream. One 12.928-Mb/s data stream is converted to four 3.232-Mb/s data streams, to use four of the five available channels of the FIFO chip.

The high speed FIFO circuit, along with timing diagrams, is shown in figure B-3. The data are strobed into the serial-to-parallel converter (54164) at the average MBS rate of 12.928 Mb/s.

At every fourth clock, the 4-bit data word is then strobed into the 74174 D-edge register. The data word is then loaded into the FIFO buffers. The 74174 register permits the data to be stable for approximately 300 ns.

The 4-bit data word is unloaded from the FIFO and strobed into the 54166 parallel-to-serial shift register. The shift/load clock for the 54166 is derived from the FIFO output clock by means of a 54161 counter and logic gates. Since the load and unload clocks of the FIFOs are asynchronous, they are derived from independent counters and logic gates.

5.3.2 Low Speed Circuit

At the two slower data rates, data are strobed into a D-edge register. The slow speed circuit is shown in figure B-2. The output of the register is strobed into the 74S225 FIFO one clock period (29 ns) later, because of the 5404 inverter (56). The propagation delay from the D to Q output of the 74S175 is 22 ns, worst case. The setup time for the 74S225 is -20 ns, providing a safety factor of 27 (20 + 29 - 22) ns. Schottky D registers are used. The setup time (data available before clock edge) is only 5 ns in the Schottky device and 25 ns in the 74S175 device.

Data are unloaded from the 74S225 by means of a separate and asynchronous unload clock. The data are buffered in a 74S175 register.

5.4 DEMULTIPLEXER BOARD

The major task of the demultiplexer board is to develop the load clock for each of the FIFOs according to the frame format and received stuff control bits. ECL is used because the clocking speed on this board is 34.368 Mb/s. As in the multiplexer board, registers are used in a pipeline configuration, to permit each chip or group of chips to have a full clock cycle for settling times. The worst case propagation time occurs in the 10549 4 by 8 PROM, with a specified worst case of 25 ns.

The demultiplexer schematic diagram is included in figure B-4 in appendix B. The received clock (CLOCK IN) is derived in the frame acquisition board (figure B-5) from the HDB3 data. The clock is distributed throughout the board by means of the 10110 (39). A modulo-256 counter (8 bits) is used to generate all the addresses to the control PROMs (27, 50, 51, and 53). During normal operation,

after frame acquisition, the counter runs free. During frame acquisition, the counter is reset to 0 and then preset to 16, under control of the frame acquisition circuit to synchronize the counter with respect to the received framing sequence. PROM (27) generates clock pulse gating signals (D_0, D_1, D_2, and D_3) for each of the four respective demultiplexer FIFOs. PROM (51) generates clock pulse gating signals for each of the four respective stuff opportunity times. The "AND" gates in position 43 enable these pulses. A pulse is enabled if the STUFF control word (3 bits for each data port) in the frame indicates a high with a majority vote. The majority vote is performed by four counters, one assigned to each port (32, 33, 44, and 45). A count greater than 2 will enable the corresponding "AND" gate in (43).

The 3 bits of each stuff control word are used as the inputs to their respective counters (32, 33, 44, and 45). The stuff control bits come from the data stream via the gates in IC (57). Each of these four gates is enabled three times in the frame by means of the PROM in location 53. The "AND" gates in position 56 are used to gate the inverted clock during the stuff control times to enable the stuff control bits to be counted. The counters operate on positive going clock edges. Since the controlling edge occurs very near the center of a data pulse, timing glitches are eliminated. The least significant bit (LSB) + 1 of the 10578 counter provides the majority vote, since that bit is high on either the count of 2 or 3. The counters are reset at the beginning of each frame.

It should be noted that the stuff control majority vote occurs in the second half of the frame, and the vote is complete before the arrival of the stuff opportunity time. Hence, the "AND" gates in IC (43) will have already been enabled by their respective majority vote counter before the stuff opportunity clock arrives. The corresponding "true" data clock and gated stuff opportunity clock are "ORed" together in IC (31) before being translated to TTL levels. The PROM in location 50 develops a pulse at time "10" in the frame count for use in the frame acquisition board.

The three tandem "OR" gates in position 59 are used to delay the data by approximately 6 ns. This prevents "ANDing" of the enabled inverted clock at the inputs to the "AND" gates of position 57 with that of the data following the stuff control bits. Narrow glitches of a few nanoseconds are thereby prevented from occurring at the trailing edge of the enabled stuff control pulse at the output of the "AND" gates in position 57.

5.5 FRAME ACQUISITION

The frame acquisition board acquires framing information and synchronizes the demultiplexer address counter with that of the incoming data stream. It continuously monitors the framing sequence time of detection with respect to the demultiplexer address counter. If the demultiplexer frame address counter is in proper registration with respect to the framing sequence, the frame acquisition board will not change the demultiplexer address counter. If, however, the address counter is not in proper registration with respect to the framing sequence, the frame acquisition board will, after two frames, force the demultiplexer address counter to be in synchronism with the received frame word.

Figure B-5 shows the circuit schematic for the frame acquisition board. The sequence of framing bits is shown in the upper center portion of the print. All data pass through a serial shift regiater (three 10141s) at locations 25, 26, and 38. When the framing bits are in the shift register with the first framing bit at Q_3 of location 38 and the last bit at Q_2 of location 25, the presence of the correct sequence, with no errors, is detected by ICa at locations 39 and 40. The presence of the frame sequence ia denoted by having pin 3 of IC (39) go high during the clock period in which the sequence is detected. If the address counter of the demultiplexer and the frame detect pulse are in synchronism, a pulse developed once per frame by the address counter, called the "10" detect pulse, will be coincident in time with the frame detect pulse. These pulses are "ANDed" together to produce a pulse at pin 2 of IC (30). The "10" detect pulse from the address counter also drives a 10178 binary counter at location 42. (After registration, the "10" detect pulse occurs at time 12 at the clock input to IC 42.) This counter (42) is reset to 0 if pin 2 of IC (30) detects the framing bits at the expected time in the frame.

If, however, framing is lost, the 10178 counter will continue to increment each frame. After three frames of incrementing, the output of the binary comparator at pin 2 of location 53 will go high, enabling the demultiplexer address counter to be forced into coincidence with the framing sequence.

Pin 3 of IC (30) first resets the demultiplexer counter to 0. The output of the digital comparator enables the gate. During the next clock interval, the address counter will be preset to 16. The value of 16 is made necessary by the fact that its "10" detect pulse is actually present at time 13 at the output of the register at location 52, and there are 3 clock delays at the shift register in location 41. The present value (16) is hardwired at the demultiplexer's address counter.

5.6 RATE SMOOTHING BOARD

The rate smoothing board consists of four independent rate smoothing circuits, one for each of the four data channels. The purpose of the rate smoothing circuit is to monitor the occupancy of the associated output FIFO circuits and automatically adjust the unload clock rate to keep the occupancy approximately half full over a long integration period. The frame format guarantees that there will be a constant amount of data, to within 1 bit, written into the FIFO at each frame period (7.4 microseconds). The long term average of the data rate will be the same as the input data rate, which is usually controlled by a crystal oscillator.

Figure B-6 shows the rate smoothing circuit. The upper left corner shows a block diagram of the canonical form of each rate smoothing circuit. The FIFO status signal is fed into a non-inverting amplifier, which adds a direct current (dc) offset of -2.5 V at the output of the signal. The purpose of the offset is to level shift the status input waveform to generate a bipolar signal. The second operational amplifier is configured as a simple integrator. The back-to-back Zener diodes are used to limit the VCXO voltage to $\pm$5 V for protection of the VCXO. The VCXO has a negative slope frequency to voltage transfer characteristic.

5.7 HDB3 ENCODER

The composite 34-Mb/s signal is encoded into HDB3 (high density binary 3) format in accordance with CCITT standard G.703. The HDB3 code is a pseudo-ternary code with three states, denoted by B+, B-, and 0. The marks are transmitted in alternate polarity; the zeros are transmitted as 0, except as noted below. The 3 indicates that the code substitutes marks in sequences of more than three consecutive zeros. The second and third zeros of a string are transmitted unchanged. The fourth zero of a string is transmitted as a mark, with the same polarity as the previous mark, thereby violating the alternate mark inversion (AMI) rule of the code. The first zero of a string of four consecutive zeros may or may not be modified to a mark, to cause successive violations of opposite polsrity. This code provides zero dc offset and facilitates clock recovery at the receiving end of the link.

The HDB3 encoder is designed to produce an HDB3 encoded signal from an NRZ signal using hardwired logic elements. At each clock interval, two digital signals are produced. One signal denotes whether the corresponding HDB3 output will be a zero or a mark. The other signal denotes the polarity of the mark. These two digital signals are then converted to HDB3 format at the very last stage of

the encoder. The major subfunctions of the encoder are to detect strings of four zeros and designate the first and fourth zero, provide for proper delay and timing registration, develop the polarity of the current violation and store the polarity of the last violation and last mark, provide logic for controlling the polarity of the marks as a function of the previous state, and lastly produce the ternary signal from the two binary signals mentioned above.

Figure B-7 shows the schematic diagrams of the encoder and decoder. The NRZ data to be encoded are clocked through a D-edge shift register (50) to detect sequences of four or more zeros by means of a "NOR" gate (51). Shift registers (38 and 39) provide compensatory delay for the main data streams. Clock pulses to drive the circuit are developed at (42), which provides clock distribution.

Marks developed by the first zero in sequences of four may be inhibited by the gate control at pin 13 of (40). (First zero marks are inhibited if the preceding mark of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself.) The "first zero mark" is "ORed" with the mark corresponding to an NRZ "one" at (41) input pins 4 and 5. The "fourth zero mark" is also ORed with the other two possible marks at input pins 13 and 12 of (41). The signal labeled A in the diagram goes high at each mark. The signal labeled B in the diagram designates the polarity of the mark. Table 1 shows the relationship between the control signals A and B and the HDB3 code.

Table 1. HDB3 Control Signal Relationship

Mark Control	Polarity Control	Output Voltage
A	B	HDB3
0	0	0
0	1	0
1	1	B+
1	0	B-

The HDB3 code is generated by steering marks to one or the other side of a center tapped transformer. The marks (A control line) are first converted to 14.55-ns pulses and then steered to the proper side of the transformer by the polarity control line (B).

5.8 HDB3 DECODER

The HDB3 decoder converts HDB3 code to NRZ. It is pictured as the top schematic in figure B-7. The board also contains a phase locked loop clock recovery circuit, to regenerate the 34.368-MHz clock in synchronism with the data.

The three-level input signal is terminated in 75 ohms at (37). Threshold detectors at position 38 convert the three-level signal into two NRZ signals, according to the waveform shown in the upper left-hand corner of the schematic diagram. The output of the "exclusive OR" gate, pin 12 of (40) goes high at each logic "one." Since the HDB3 format is guaranteed not to have more than three "zeros" in a row, a clock edge can be generated at "zero" locations by having the signal pass through a four-tap delay line with tap spacings of 29 ns (57). The outputs are "ORed" together to produce a 34.368-MHz clock signal with jitter, because the delay line lengths are not accurate. The crystal controlled phase locked loop removes the jitter. The phase locked loop uses a linear phase detector, an RC low pass filter, and an operational amplifier error integrator. The "jitter free" 34-MHz clock is used to drive the decoder circuit via the clock distribution IC at location 30. The outputs of the two threshold detectors at position 38 are registered by the D-register at location 39, with the strobe clock occurring at the center of the detected pulse.

The key logic waveforms in the decoder are described: Pin 2 of IC (40) goes high at each mark. Pin 3 of IC (42) goes low after a violation for the duration of the violation. The circuit detects two adjacent marks with the same polarity. The D-registers at (41) are clocked only during mark intervals, and the polarity of two successive marks are compared in the "exclusive OR" gate at (40).

The violation detection causes a mark to be inhibited at time t_0 and t_3. IC (31) is the shift register delay line and IC (44) provides the gates for the inhibit line.

5.9 BITE BOARD

The BITE logic board schematic diagram is shown in figure B-8. The BITE board in no way affects the operations of the system. Failure of the BITE logic will not cause a failure in the system. This board monitors all the power supply voltages (+12, -12, +5, -5, and -2) used in the system. A Zener diode at location 26, along with voltage divider resisters, generates two reference voltages at 3.5 and 3.0 V. Similarly, a Zener diode at location 38 and a voltage divider generate reference voltages at -3.5 and -3.0 V, and

another set of reference voltages at -1.7 and -1.5 V. The +12 and +5 V power supply voltages are divided down to +3.25 V. The -12 and -5 V power supply voltages are divided down to -3.25 V. A pair of comparators is used for each power supply voltage test. For example, the voltage comparators at location 27 are used to test the +12 V power supply. The +3.5 V reference is applied at pin 14, and the nominal +3.25 V signal is applied at inverting input pin 15. The output (pin 1) is high as long as the voltage at pin 15 is less than that of pin 14. Similarly, at the other comparator of package 27, a +3 V reference signal is applied to pin 6 (inverting), and the nominal 3.25 signal is applied to pin 5. The output (pin 10) is high as long as the voltage at pin 5 is greater than the voltage at pin 6. A high from both comparators indicates that the nominal signal voltage is greater than +3.0 V and less than 3.5 V. The comparators in locations 39, 40, 51, and 52 are used to test the +5, -5, -2, and -12 V power supply voltages. The outputs of all comparators are "ANDed" via a pyramid structure, using the "AND" gates in locations 28, 53, and 29, to form a signal that indicates the status of the power supply voltages. If all the power supply voltages are within tolerance, pin 10 of IC (29) will go high.

The half-full status lines for each data rate at both multiplexer and demultiplexer FIFOs are registered four times each frame by the D-edge registers in positions 1 and 10. At the output of each register, there is a 74123 retriggerable monostable multivibrator (positions 14, 13, 22, and 21). The resisters and capacitors in positions 2 and 9 set the time constants, approximately 50 microseconds each, for each of the multivibrators. When the status line is active (constantly changes state), the output of the corresponding retriggerable multivibrator will remain high. A logic high will turn off the corresponding indicator light of the front panel. The light driver is an open collector 7416 inverting driver. Between the logic control circuitry and each of the light emitting diode (LED) drivers, there is an "AND" gate, controlled by the LED (Lamp) TEST button.

The frame status indicator is active when the demultiplexer has acquired framing. At the frame acquisition circuit board, the output of the "AND" gate that detects the coincidence of the detect "10" pulse of the demultiplexer addresa counter and the framing sequence detect pulse is used to drive a retriggerable monostable multivibrator, whose period is 10 microseconds. Because the frame length is 7.4 ns, the multivibrator will always be high when the system acquires framing. The output of the frame acquisition retriggerable multivibrator is also used as an input to a set-reset flip-flop at location 31. IC (32) is used as the LED test gate and IC (33) is used as the LED driver.

The BITE board also contains a summary status line at pin 10 of IC (17).

5.10 TEST EMULATOR

The test emulator board is shown in figure B-9. Although not part of the working system, a test emulator board has been made to simulate clock and data at all data rates. Crystal oscillators are used to generate the clock, and counters driven by the respective oscillators are used to generate data.

A 3.072-MHz oscillator has its output divided by 16 to generate the 192-kb/s clock. Further frequency division by another 74161 counter generates the simulated data. Two oscillators and frequency counter chips are used to generate asynchronous clock and data signals at 12.928 Mb/s. Another crystal oscillator and divider is used to generate the signals for the 2.048-Mb/s data source.

Crystal oscillators were used in the simulator board to ensure that frequency limits are within the capture ranges of the voltage controlled oscillators of the rate smoothing circuit. The frequency divider outputs used to simulate data are pin selectable, with outputs of 1/2, 1/4, 1/8, and 1/16 the input clock rate.

The test emulator board can be used to test most aspects of the entire system. The simulator can test multiplexer and demultiplexer BITE functions. Similarly, the overall system jitter can be viewed on an oscilloscope, by comparing the input signal generated by the simulator with that of the output of the rate smoothing board.

5.11 FRONT PANEL INDICATORS

The BITE board monitors key signal parameters of the rate converter to provide system status via the front panel. In general, the green lights should always be activated when the system is operating satisfactorily. The red lights indicate abnormal conditions. The yellow lights indicate conditional faults that require interpretation, based on past history. Under the POWER heading, there are two fault indicators: a green light labeled BITE and a yellow light labeled FAULT. The green light (active) indicates that +5 V is being brought to the BITE board. The yellow light (active) indicates that one of the power supplies is not within tolerance ($\pm$10%). The power supply voltage can be read at the test point associated with each power supply at the power supply front panel.

The two yellow lights labeled SPARE 1 and SPARE 2 are not wired.

There are eight FIFO status indicators, corresponding to each data channel in the multiplexer and in the demultiplexer. These status indicators monitor activity of the half-full sense lines on the FIFOs. When the system is working properly, the occupancy at each FIFO will vary continuously about the half-full condition. Lack of activity will indicate improper operation and will be designated by a red light.

If the demultiplexer has acquired framing, the green FRAME LOCK light will remain on. The point monitored for this indicator is the output of gate (30) pin 2 of the frame acquisition board. This gate goes high when the "10" detect pulse from the demultiplexer counter is coincident with the framing sequence detect pulse.

Failure to detect framing will set a latch (IC 30 in the BITE logic board) that activates the FRAME SEARCH indicator (yellow). Pushing the reset button will reset and shut off the light.

The LED TEST button is used to test all front panel status lights.

BIBLIOGRAPHY

1. Spilker, J. J., "Digital Communications by Satellite," New Jersey: Prentice Hall Inc., 1977.

2. The International Telegraph and Telephone Consultative Committee (CCITT), "Recommendation G.703," Vol. III.2, International Telecommunication Union, Geneva, 1977, pp. 400-407.

APPENDIX A

FRAME STRUCTURE

There are 256 clocking intervals in the frame. Each interval is defined and listed according to the following notation:

Notation	Index	Definition
Fj	$0 \leq j \leq 9$	Frame Bit
Alarm		Count 10 in Frame (not used)
National		Count 11 in Frame (not used)
Lj	$0 \leq j \leq 14$	CEPT Level 1 Data Bits
STLj	$1 \leq j \leq 3$	CEPT Level 1 Stuff Control Bits
LS		CEPT Level 1 Stuff Position (247)
MAj	$0 \leq j \leq 95$	A-Mission Bit Stream Data Bits
STAj	$1 \leq j \leq 3$	A-Mission Bit Stream Stuff Control Bits
MAS		A-Mission Bit Stream Stuff Bit Position (254)
MBj	$0 \leq j \leq 95$	B-Mission Bit Stream Data Bits
STBj	$1 \leq j \leq 3$	B-Mission Bit Stream Stuff Control Bits
MBS		B-Mission Bit Stream Stuff Bit Position (255)
SCO		Service Channel Bit Stream Data Bit (116)
STSj	$1 \leq j \leq 3$	Service Channel Bit Stream Stuff Control Bits
SCS		Service Channel Bit Stream Stuff Bit Position (244)

The frame usage is shown in table A-1.

Table A-1. Frame Usage

Count	Bit Type	Count	Bit Type
0	F1 (1)	43	MA14
1	F2 (1)	44	MB14
2	F3 (1)	45	MA15
3	F4 (1)	46	MB15
4	F5 (0)	47	MA16
5	F6 (1)	48	MB16
6	F7 (0)	49	MA17
7	F8 (0)	50	MB17
8	F9 (0)	51	MA18
9	F10 (0)	52	MB18
10	Not Used (Alarm)	53	L3
11	Not Used (National)	54	MA19
12	MA0	55	MB19
13	MB0	56	MA20
14	L0	57	MB20
15	MA1	58	MA21
16	MB1	59	MB21
17	MA2	60	MA22
18	MB2	61	MB22
19	MA3	62	MA23
20	MB3	63	MB23
21	MA4	64	L4
22	MB4	65	MA24
23	MA5	66	MB24
24	MB5	67	MA25
25	L1	68	MB25
26	MA6	69	MA26
27	MB6	70	MB26
28	MA7	71	--
29	MB7	72	MA27
30	MA8	73	MB27
31	MB8	74	--
32	MA9	75	MA28
33	MB9	76	MB28
34	MA10	77	MA29
35	MB10	78	MB29
36	MA11	79	L5
37	MB11	80	MA30
38	MA12	81	MB30
39	MB12	82	--
40	L2	83	MA31
41	MA13	84	MB31
42	MB13	85	MA32

Table A-1. (Continued)

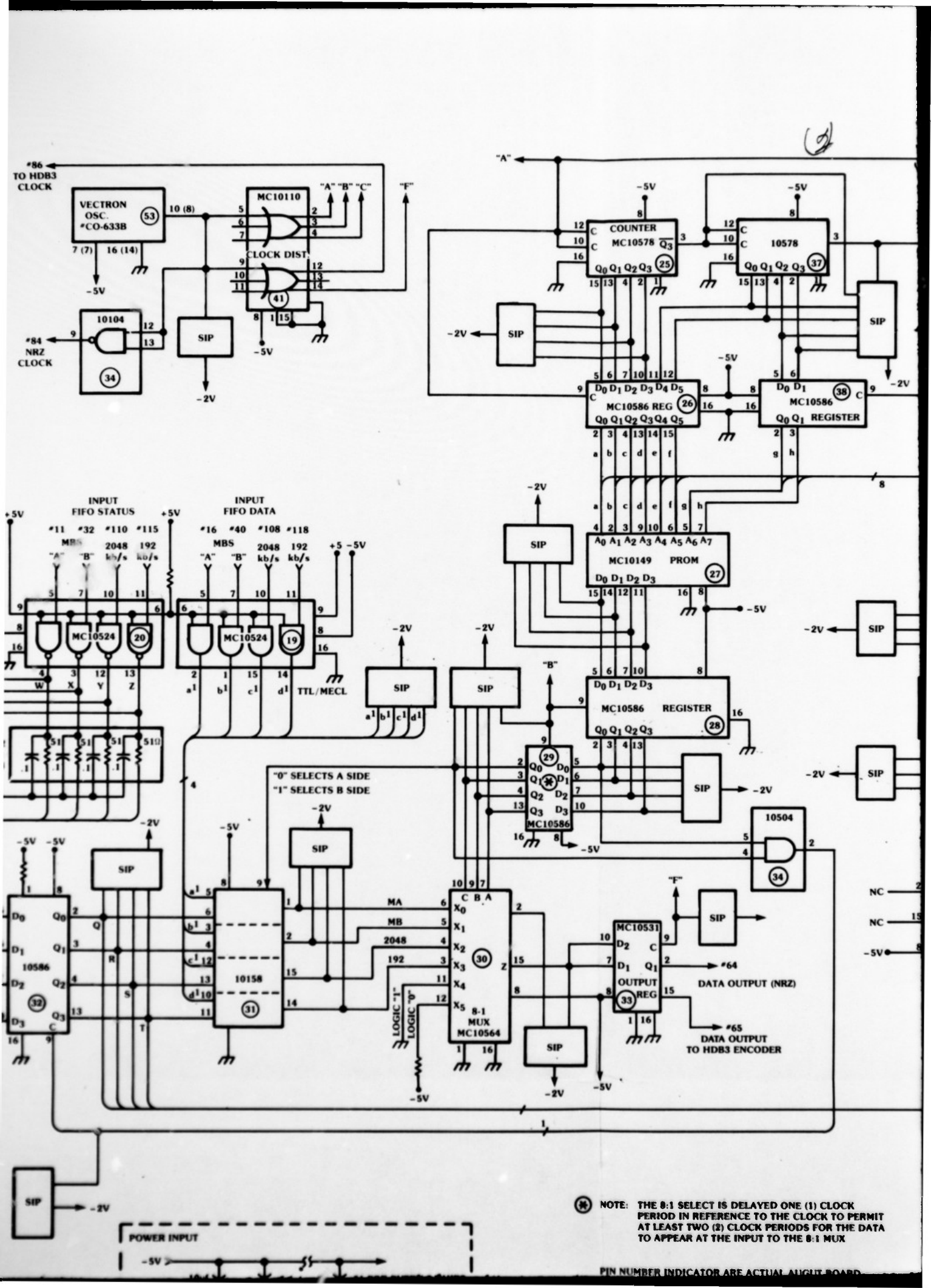
Count	Bit Type
86	MB32
87	--
88	MA33
89	MB33
90	--
91	MA34
92	MB34
93	MA35
94	MB35
95	L6
96	MA36
97	MB36
98	-
99	MA37
100	MB37
101	MA38
102	MB38
103	--
104	MA39
105	MB39
106	--
107	MA40
108	MB40
109	MA41
110	MB41
111	L7
112	MA42
113	MB42
114	MA43
115	MB43
116	SC0
117	MA44
118	MB44
119	--
120	MA45
121	MB45
122	MA46
123	MB46
124	--
125	MA47
126	MB47
127	L8
128	MA48
129	MB48
130	MA49
131	MB49
132	--
133	MA50
134	MB50
135	--
136	MA51
137	MB51
138	MA52
139	MB52
140	STS1
141	MA53
142	MB53
143	L9
144	MA54
145	MB54
146	MA55
147	MB55
148	STS2
149	MA56
150	MB56
151	MA57
152	MB57
153	STS3
154	MA58
155	MB58
156	--
157	MA59
158	MB59
159	MA60
160	MB60
161	L10
162	MA61
163	MB61
164	--
165	MA62
166	MB62
167	STL1
168	MA63
169	MB63
170	MA64
171	MB64

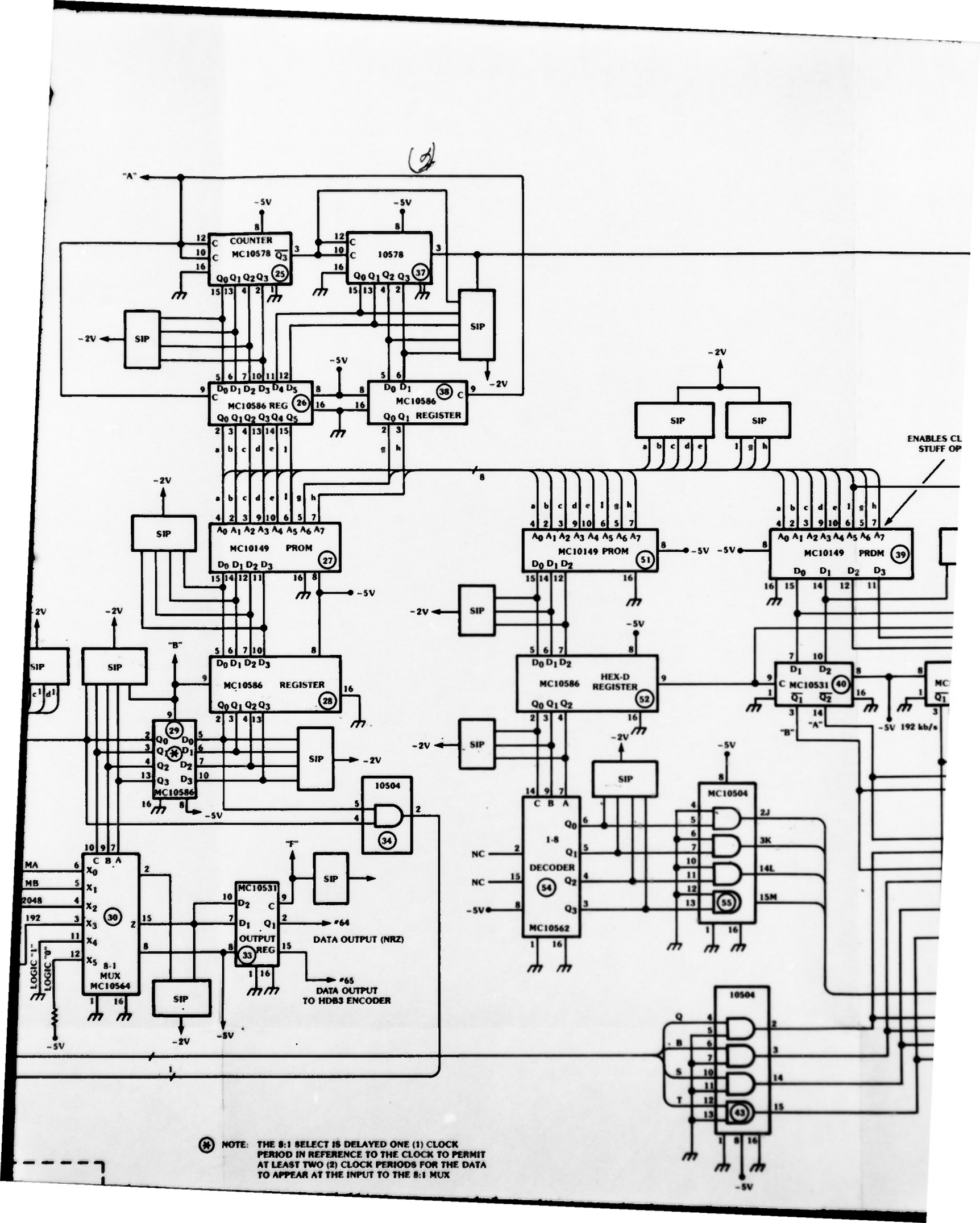
Table A-1. (Concluded)

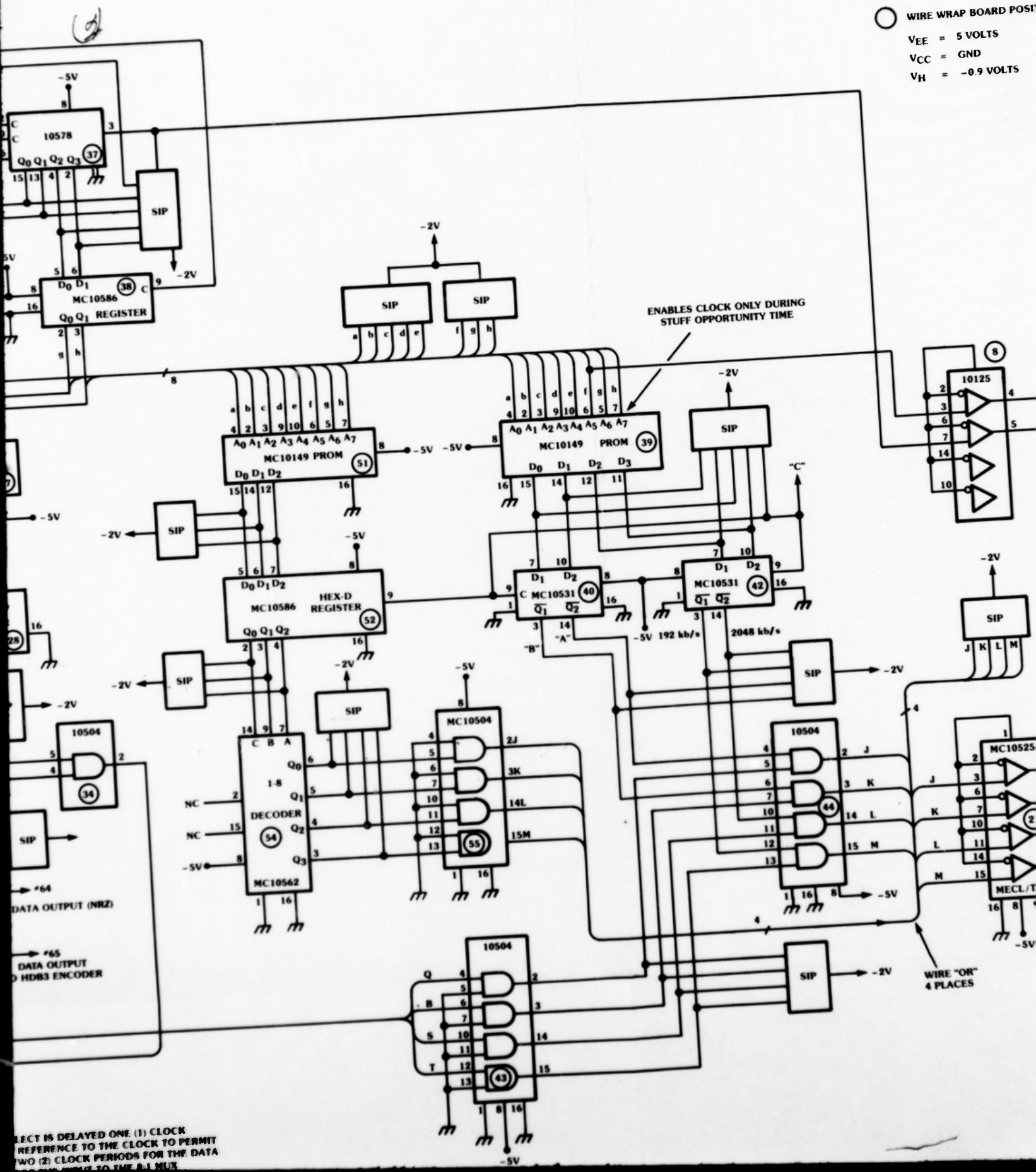
Count	Bit Type
172	STL2
173	MA65
174	MB65
175	STL3
176	MA66
177	MB66
178	MA67
179	MB67
180	L11
181	MA68
	182MB68
183	--
184	MA69
185	MB69
186	MA70
187	MB70
188	--
189	MA71
190	MB71
191	STB1
192	MA72
193	MB72
194	MA73
195	MB73
196	L12
197	MA74
198	MB74
199	STB2
200	MA75
201	MB75
202	MA76
203	MB76
204	STB3
205	MA77
206	MB77
207	--
208	MA78
209	MB78
210	MA79
211	MB79
212	--
213	MA80
214	MB80
215	STA1
216	MA81
217	MB81
218	MA82
219	MB82
220	L13
221	MA83
222	MB83
223	STA2
224	MA84
225	MB84
226	MA85
227	MB85
228	STA3
229	MA86
230	MB86
231	--
232	MA87
233	MB87
234	MA88
235	MB88
236	L14
237	MA89
238	MB89
239	--
240	MA90
241	MB90
242	MA91
243	MB91
244	SCS
245	MA92
246	MB92
247	LS
248	MA93
249	MB93
250	MA94
251	MB94
252	MA95
253	MB95
254	MAS
255	MBS

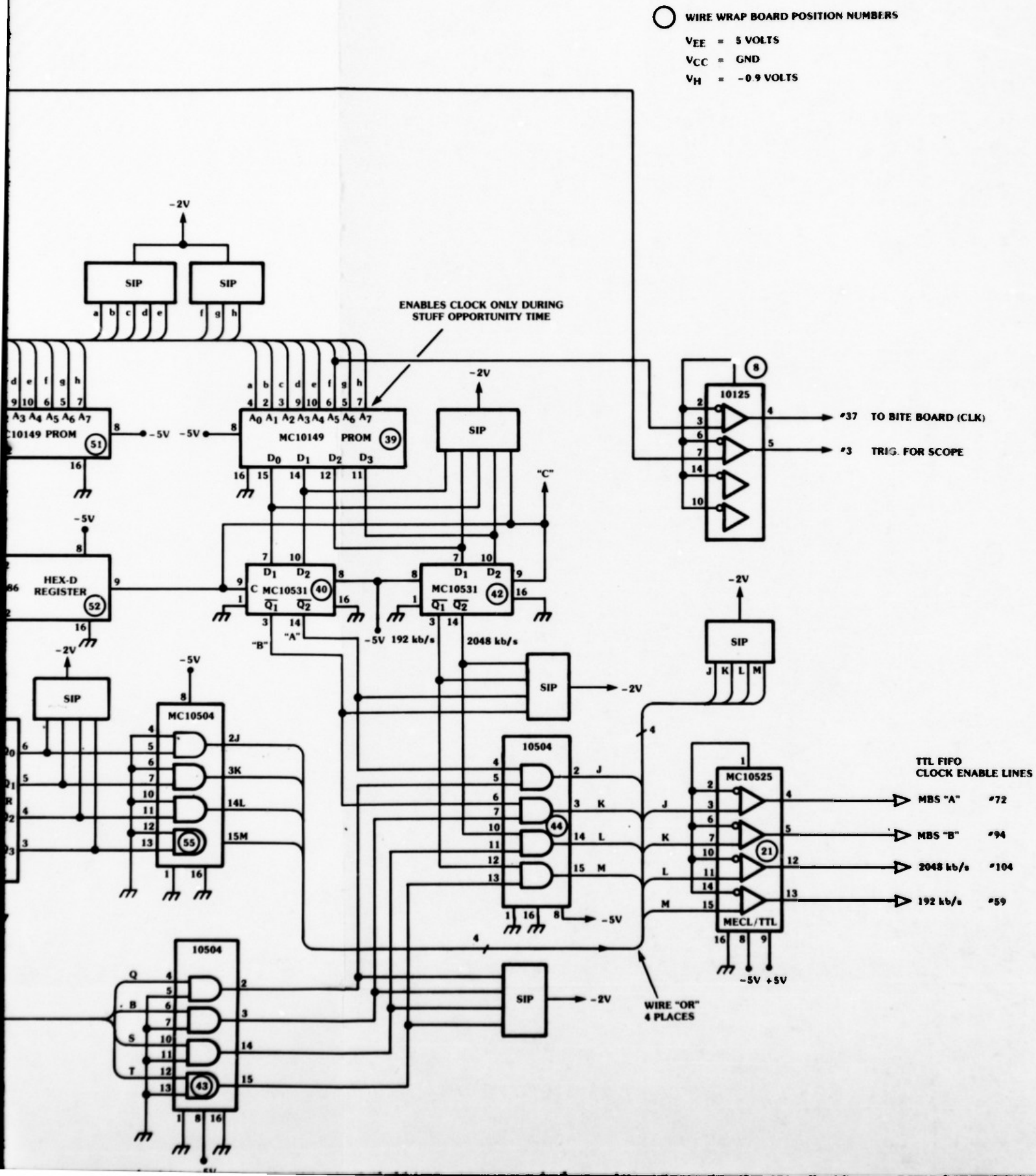
APPENDIX B

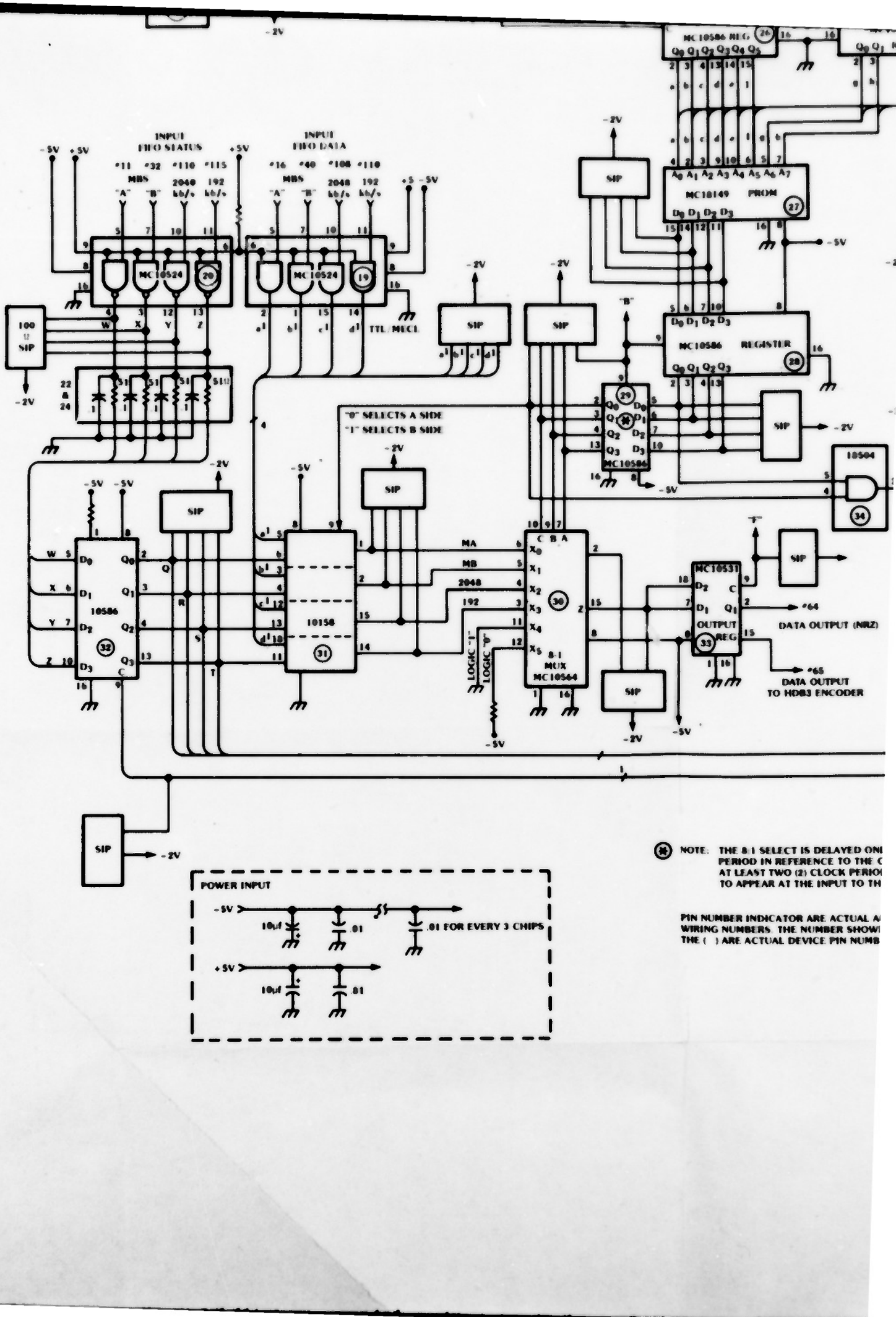
SCHEMATIC DIAGRAMS


#86 TO HDB3 CLOCK
VECTRON OSC. #CO-633B
53
10 (8)
7 (7)
16 (14)
-5V
MC10110
"A" "B" "C"
"F"
CLOCK DIST.
41
10104
34
#84 NRZ CLOCK
SIP
-2V
"A"
COUNTER MC10578
25
10578
37
MC10586 REG
26
MC10586 REGISTER
38
INPUT FIFO STATUS
#11 #32 #110 #115
MBS "A" "B"
2048 kb/s
192 kb/s
INPUT FIFO DATA
#16 #40 #108 #118
+5V
MC10524
20
19
TTL/MECL
51Ω
MC10149 PROM
27
"B"
MC10586 REGISTER
28
29
MC10586
"0" SELECTS A SIDE
"1" SELECTS B SIDE
10504
34
10586
32
10158
31
MA
MB
2048
192
LOGIC "1"
LOGIC "0"
8-1 MUX MC10564
30
MC10531 OUTPUT REG
33
#64
DATA OUTPUT (NRZ)
#65
DATA OUTPUT TO HDB3 ENCODER
NC
POWER INPUT
NOTE: THE 8:1 SELECT IS DELAYED ONE (1) CLOCK PERIOD IN REFERENCE TO THE CLOCK TO PERMIT AT LEAST TWO (2) CLOCK PERIODS FOR THE DATA TO APPEAR AT THE INPUT TO THE 8:1 MUX
PIN NUMBER INDICATOR ARE ACTUAL AUGUT BOARD


"A"
-5V
COUNTER
MC10578
25
10578
37
SIP
-2V
MC10586 REG
26
MC10586
REGISTER
38
MC10149
PROM
27
MC10149 PROM
51
MC10149
PRDM
39
"B"
MC10586
REGISTER
28
HEX-D
REGISTER
52
MC10531
40
"A"
"B"
-5V 192 kb/s
29
MC10586
10504
34
MA
MB
2048
192
LOGIC "1"
LOGIC "0"
8-1
MUX
MC10564
30
"F"
MC10531
OUTPUT
REG
33
#64
DATA OUTPUT (NRZ)
#65
DATA OUTPUT
TO HDB3 ENCODER
NC
1-8
DECODER
MC10562
54
MC10504
55
2J
3K
14L
15M
10504
43
ENABLES CL
STUFF OP
NOTE: THE 8:1 SELECT IS DELAYED ONE (1) CLOCK PERIOD IN REFERENCE TO THE CLOCK TO PERMIT AT LEAST TWO (2) CLOCK PERIODS FOR THE DATA TO APPEAR AT THE INPUT TO THE 8:1 MUX


WIRE WRAP BOARD POSIT
V_{EE} = 5 VOLTS
V_{CC} = GND
V_H = −0.9 VOLTS
ENABLES CLOCK ONLY DURING STUFF OPPORTUNITY TIME
10578
MC10586 REGISTER
MC10149 PROM
MC10586 HEX-D REGISTER
MC10531
10504
MC10504
1-8 DECODER
MC10562
10125
MC10525
SIP
WIRE "OR" 4 PLACES
192 kb/s
2048 kb/s
DATA OUTPUT (NRZ)
DATA OUTPUT
HDB3 ENCODER
ECT IS DELAYED ONE (1) CLOCK
REFERENCE TO THE CLOCK TO PERMIT
WO (2) CLOCK PERIODS FOR THE DATA


WIRE WRAP BOARD POSITION NUMBERS
V_{EE} = 5 VOLTS
V_{CC} = GND
V_H = -0.9 VOLTS
-2V
SIP
SIP
ENABLES CLOCK ONLY DURING STUFF OPPORTUNITY TIME
10125
#37 TO BITE BOARD (CLK)
#3 TRIG. FOR SCOPE
MC10149 PROM (51)
MC10149 PROM (39)
-5V
"C"
HEX-D REGISTER (52)
MC10531 (40)
MC10531 (42)
"B"
"A"
-5V 192 kb/s
2048 kb/s
MC10504
MC10504 (44)
MC10504 (55)
MC10504 (43)
MC10525
MECL/TTL
TTL FIFO CLOCK ENABLE LINES
MBS "A" #72
MBS "B" #94
2048 kb/s #104
192 kb/s #59
-5V +5V
WIRE "OR" 4 PLACES


INPUT FIFO STATUS
INPUT FIFO DATA
MBS "A" "B" 2048 kb/s 192 kb/s
MC10524
MC10586 REG
MC18149 PROM
MC10586 REGISTER
MC10586
10158
MC10564
8:1 MUX
MC10531 OUTPUT REG
10504
100 Ω SIP
TTL/MECL
"0" SELECTS A SIDE
"1" SELECTS B SIDE
MA
MB
2048
192
LOGIC "1"
LOGIC "0"
DATA OUTPUT (NRZ)
DATA OUTPUT TO HDB3 ENCODER
POWER INPUT
10µf
.01
.01 FOR EVERY 3 CHIPS
NOTE: THE 8:1 SELECT IS DELAYED ONE
PERIOD IN REFERENCE TO THE C
AT LEAST TWO (2) CLOCK PERIO
TO APPEAR AT THE INPUT TO TH
PIN NUMBER INDICATOR ARE ACTUAL A
WIRING NUMBERS. THE NUMBER SHOW
THE ( ) ARE ACTUAL DEVICE PIN NUMB

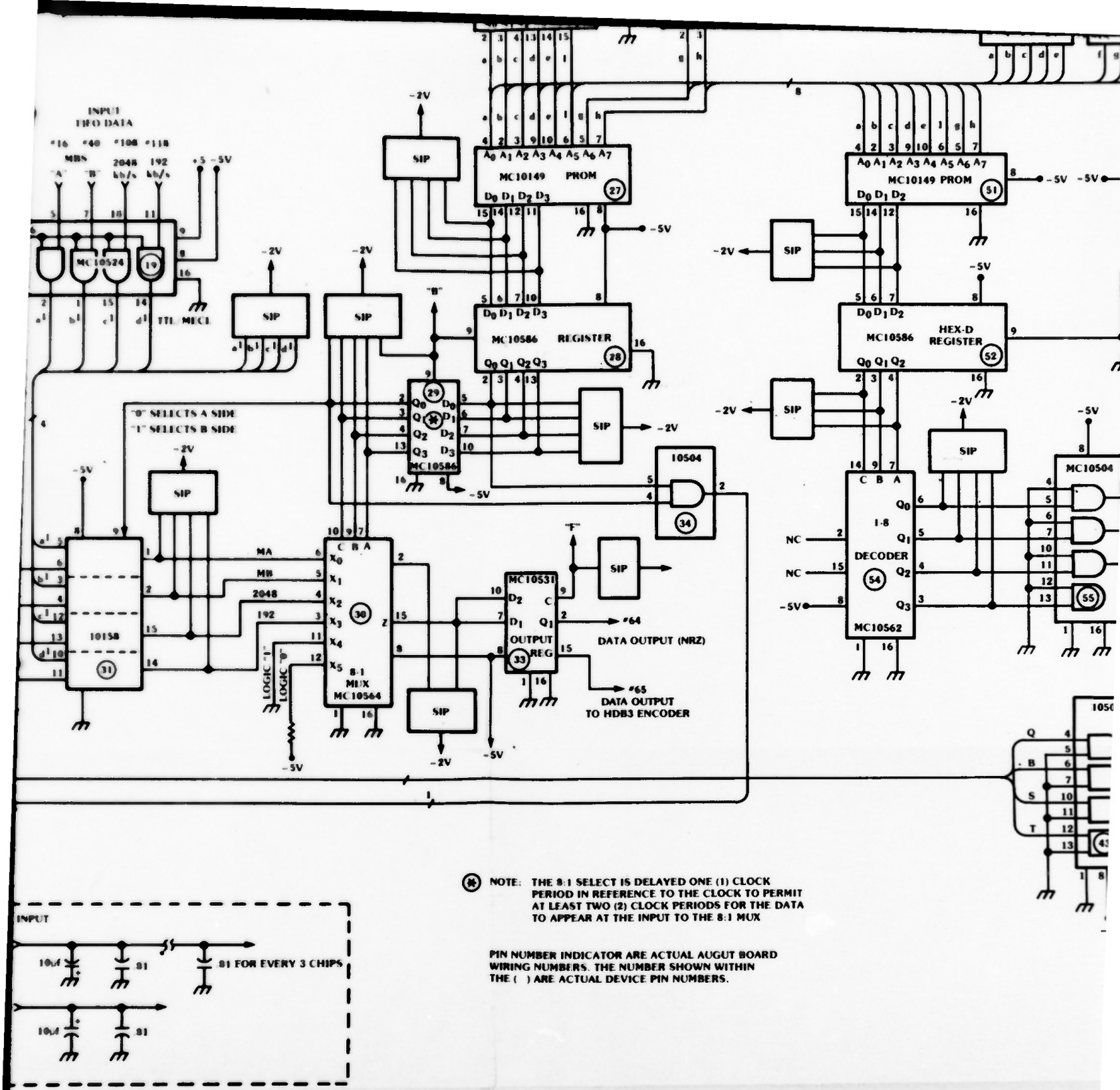
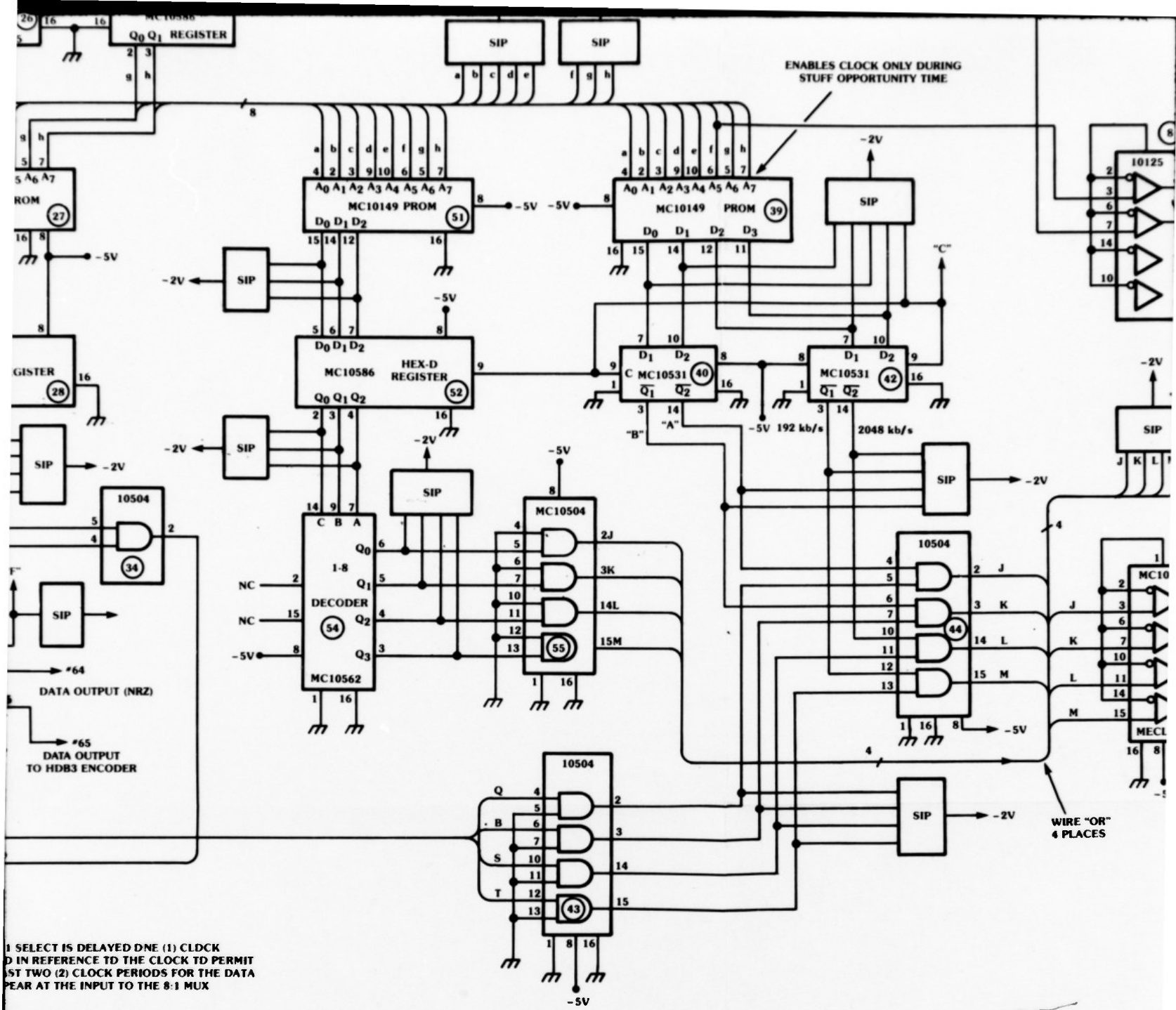


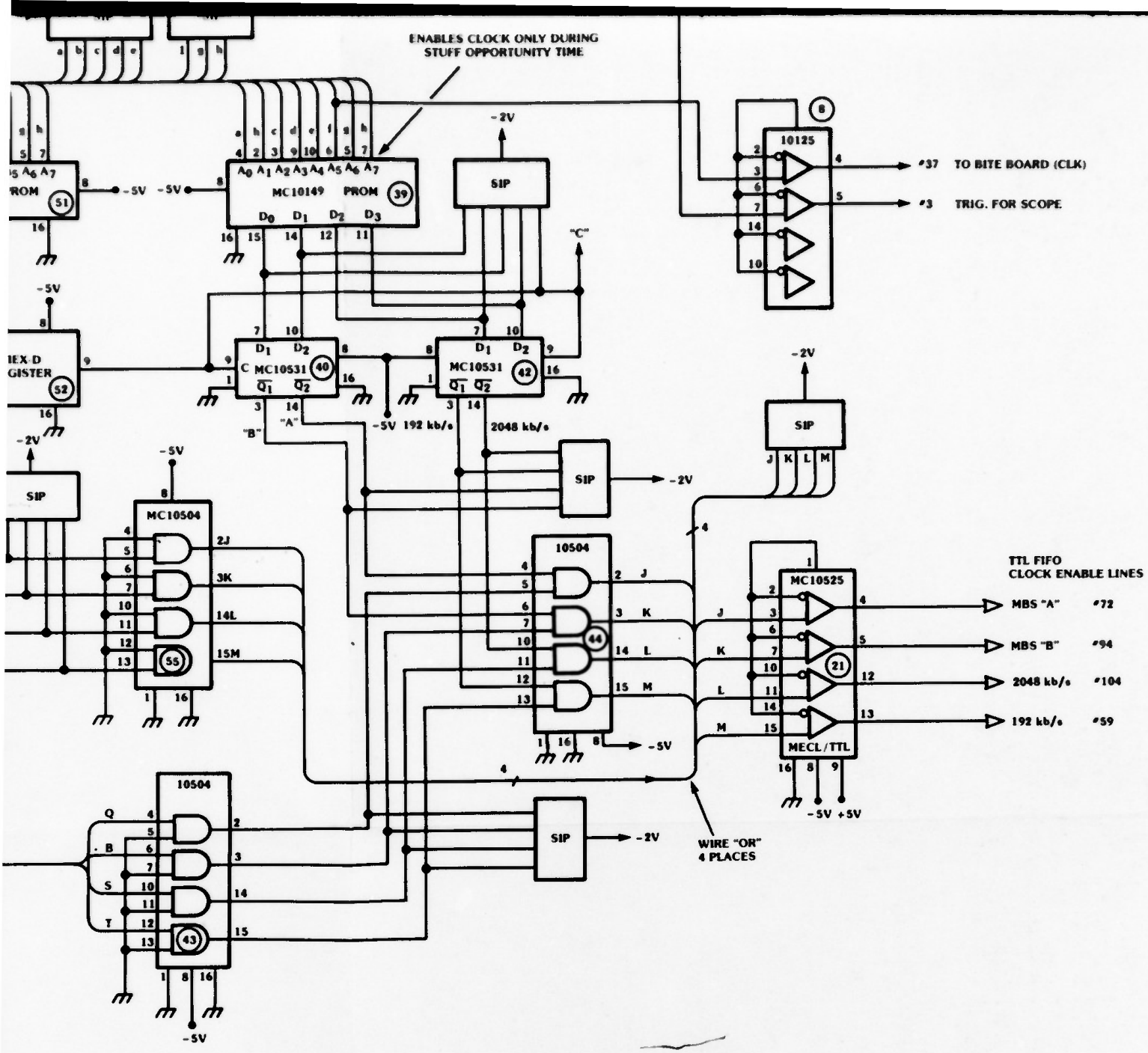
Figure B-1. MULTIPLEXER



1 SELECT IS DELAYED ONE (1) CLOCK
D IN REFERENCE TO THE CLOCK TO PERMIT
ST TWO (2) CLOCK PERIODS FOR THE DATA
PEAR AT THE INPUT TO THE 8:1 MUX

NDICATOR ARE ACTUAL AUGUT BOARD
ERS. THE NUMBER SHOWN WITHIN
CTUAL DEVICE PIN NUMBERS.

Figure B-1. MULTIPLEXER


ENABLES CLOCK ONLY DURING STUFF OPPORTUNITY TIME
-2V
-5V
MC10149 PROM
SIP
10125
#37 TO BITE BOARD (CLK)
#3 TRIG. FOR SCOPE
"C"
MC10531
"A"
"B"
192 kb/s
2048 kb/s
MC10504
10504
MC10525
MECL/TTL
TTL FIFO CLOCK ENABLE LINES
MBS "A" #72
MBS "B" #94
2048 kb/s #104
192 kb/s #59
WIRE "OR" 4 PLACES
+5V

LEXER

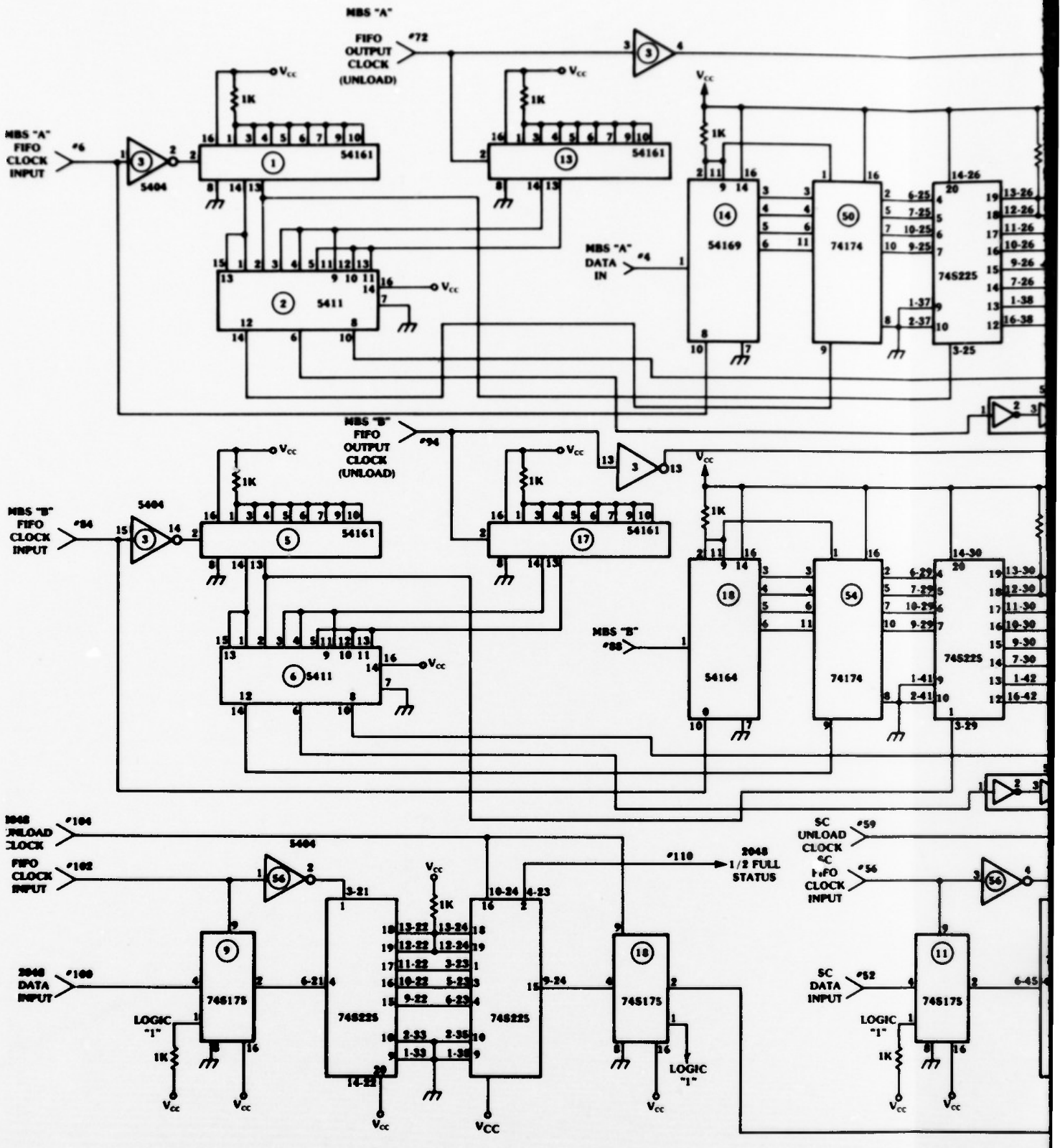
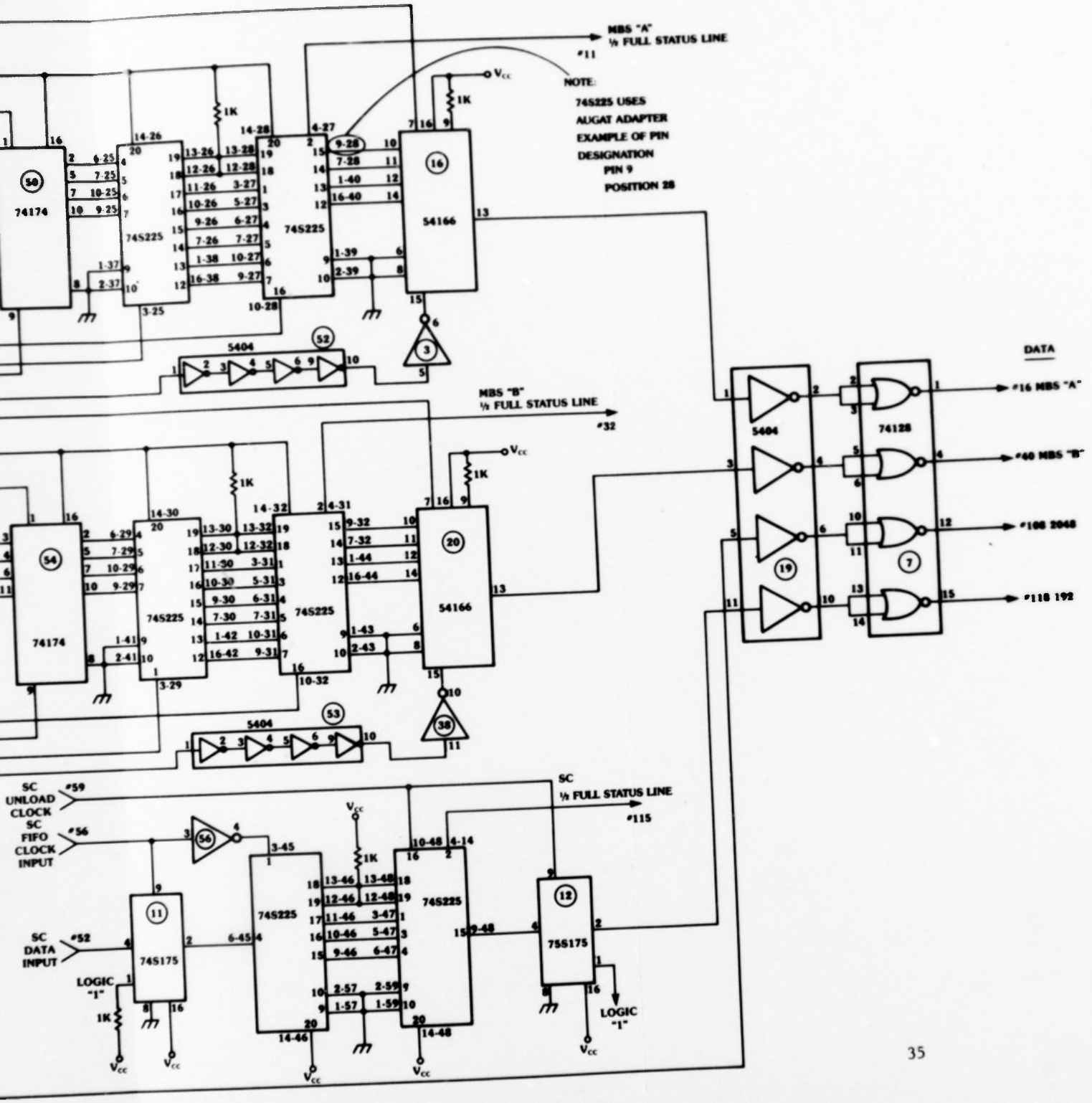


Figure B-2. FIFO BOARD (COMPLE



re B-2. FIFO BOARD (COMPLETE)

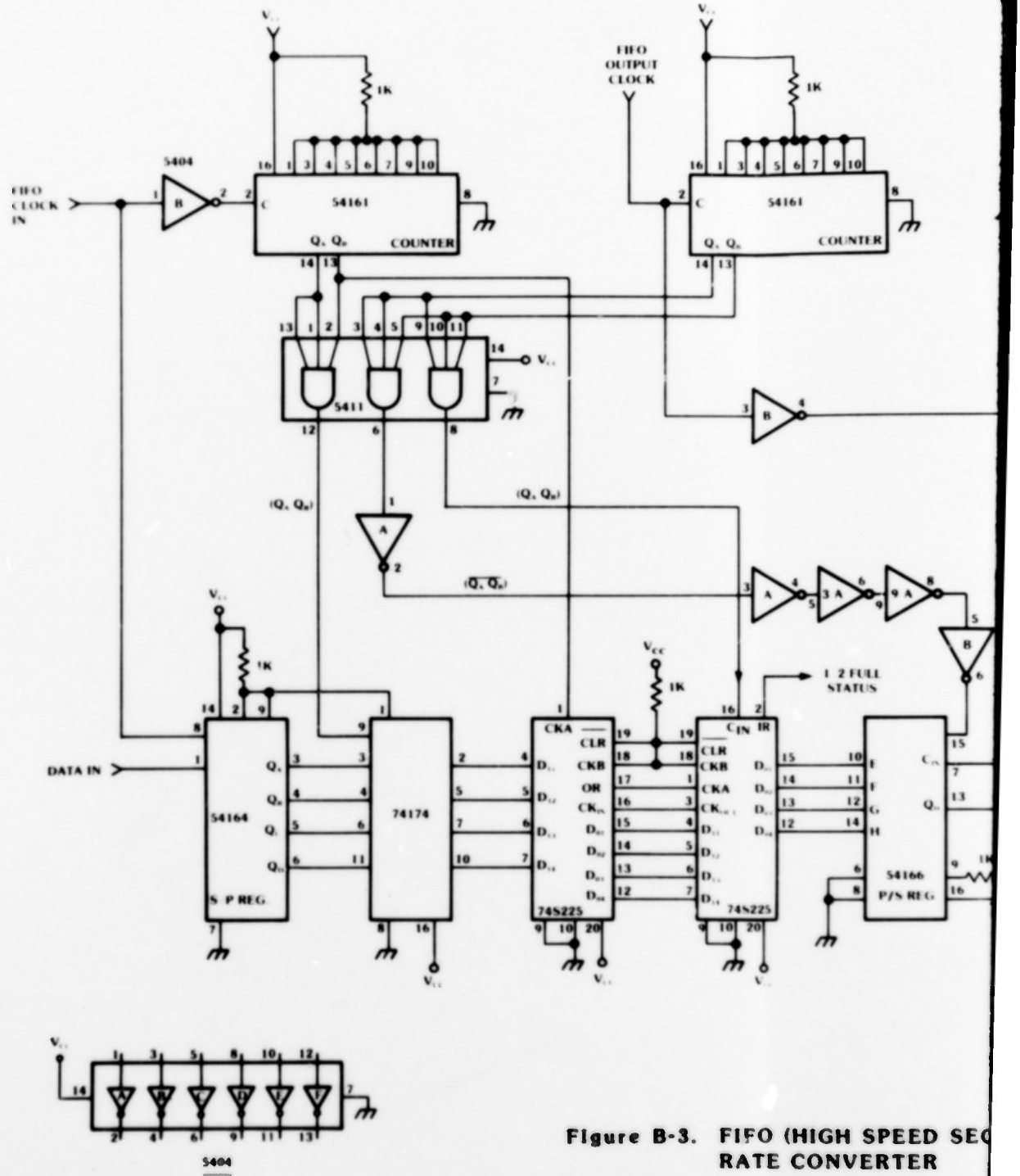
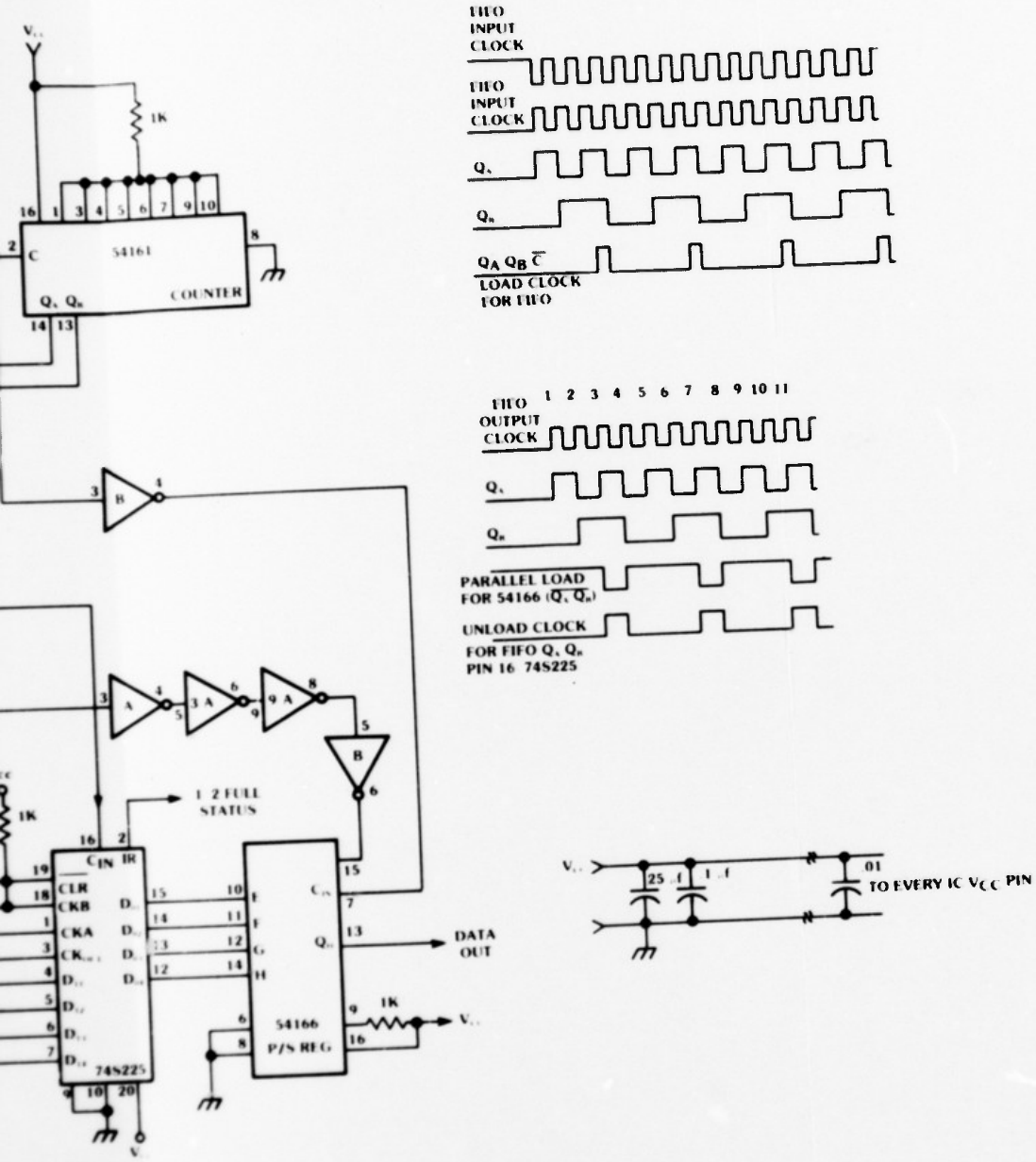
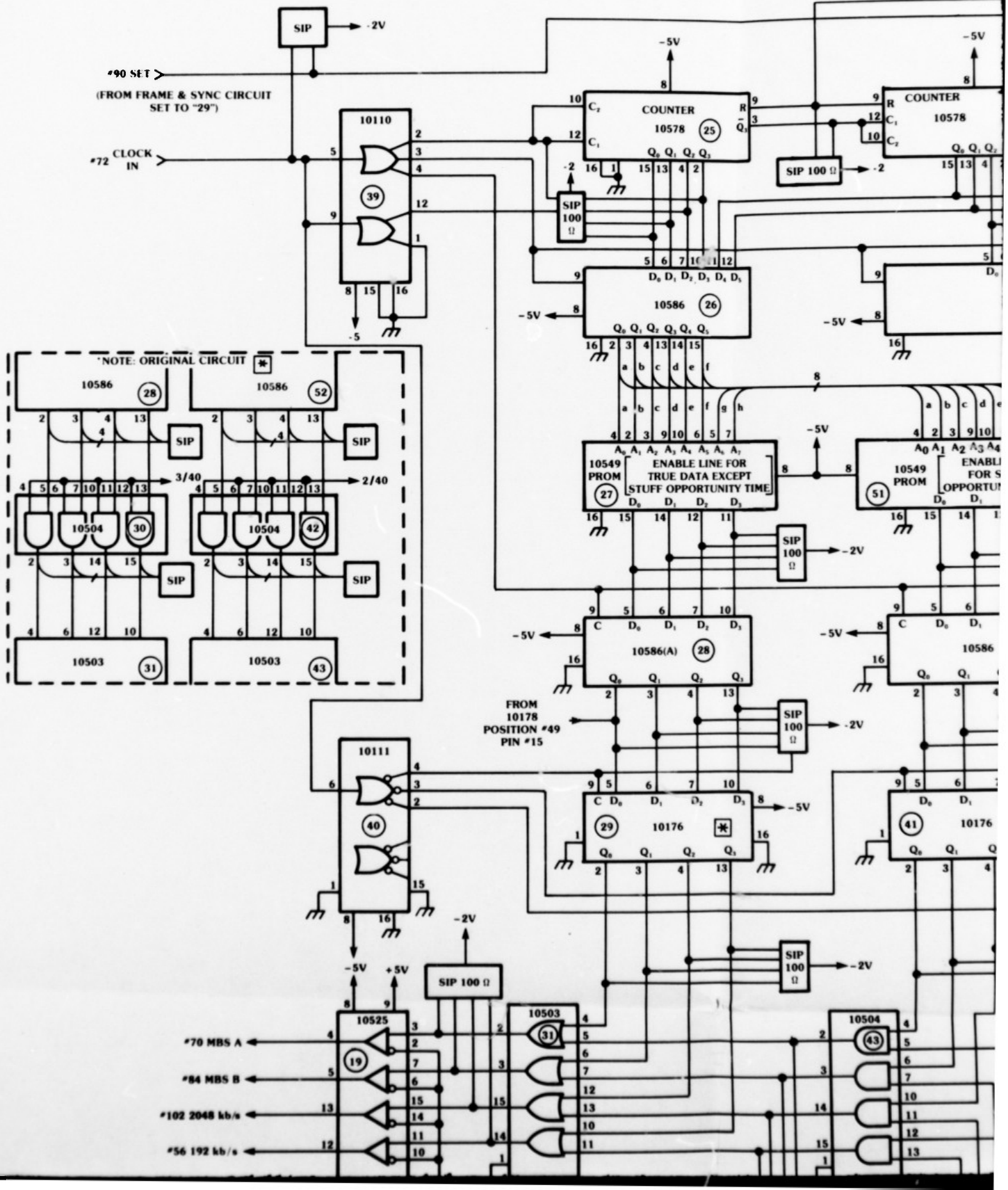
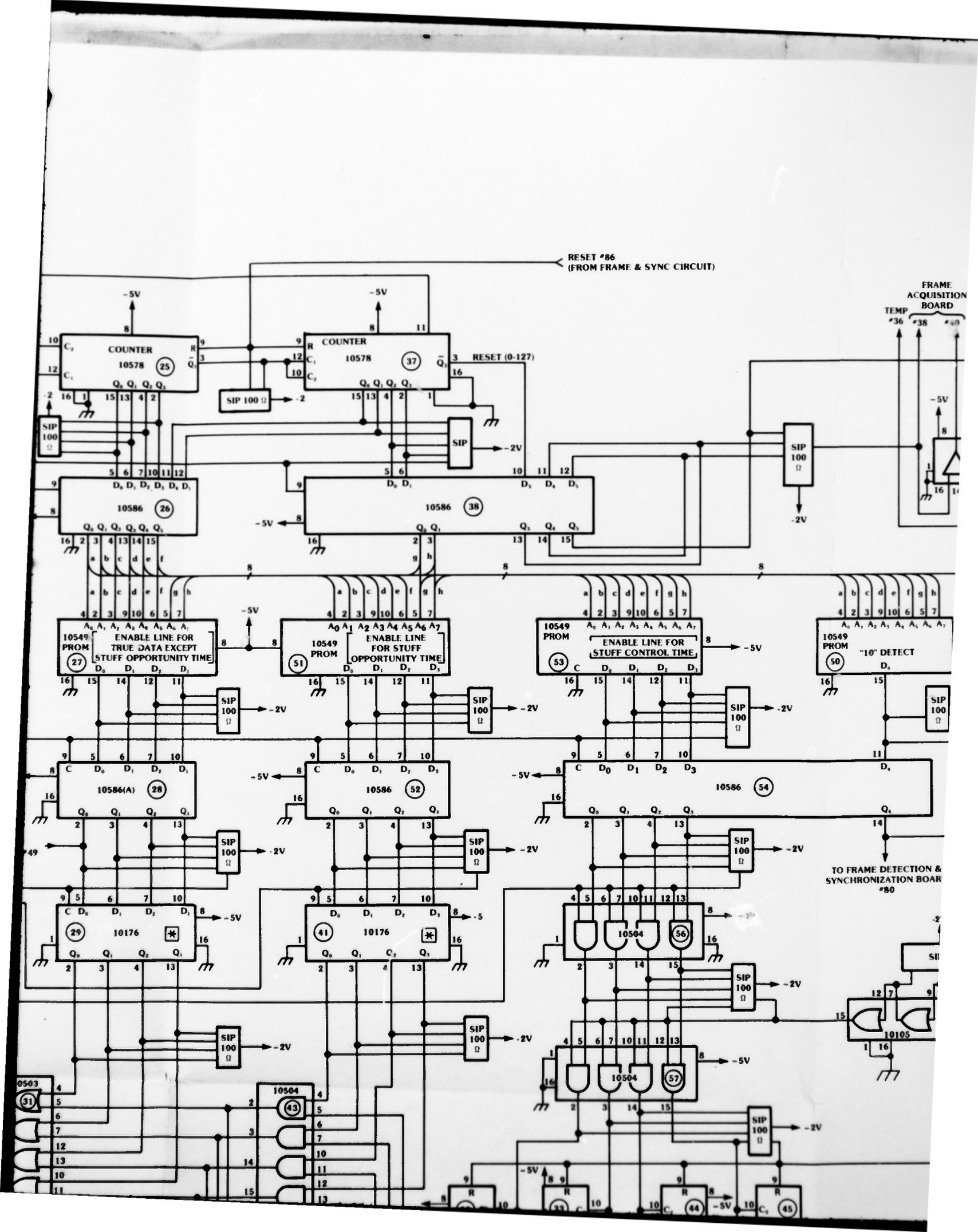


Figure B-3. FIFO (HIGH SPEED SEQ RATE CONVERTER

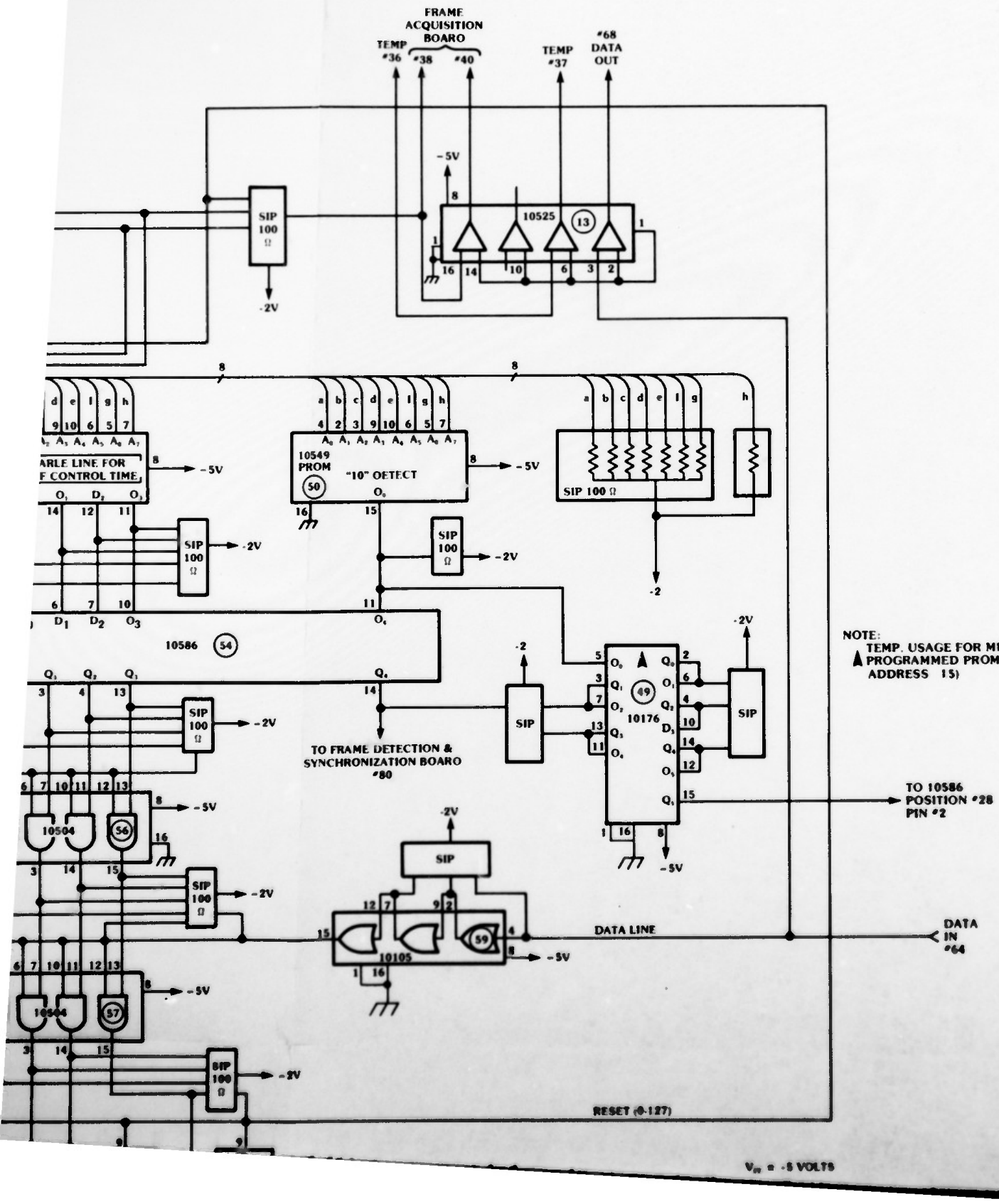


B-3. FIFO (HIGH SPEED SECTION) RATE CONVERTER


SIP
-2V
#90 SET
(FROM FRAME & SYNC CIRCUIT SET TO "29")
#72 CLOCK IN
10110
39
-5V
COUNTER
10578
25
SIP 100 Ω
10586
26
10549 PROM
27
ENABLE LINE FOR TRUE DATA EXCEPT STUFF OPPORTUNITY TIME
51
*NOTE: ORIGINAL CIRCUIT
10586
28
52
SIP
3/40
2/40
10504
30
42
10503
31
43
10586(A)
28
FROM 10178 POSITION #49 PIN #15
10111
40
10176
29
41
+5V
10525
19
#70 MBS A
#84 MBS B
#102 2048 kb/s
#56 192 kb/s
10503
31
10504
43


RESET #86
(FROM FRAME & SYNC CIRCUIT)
FRAME ACQUISITION BOARD
TEMP #36
#38
#40
-5V
COUNTER
10578
25
37
RESET (0-127)
SIP 100 Ω
-2
SIP
-2V
10586
26
38
54
10549 PROM
27
51
53
50
ENABLE LINE FOR TRUE DATA EXCEPT STUFF OPPORTUNITY TIME
ENABLE LINE FOR STUFF OPPORTUNITY TIME
ENABLE LINE FOR STUFF CONTROL TIME
"10" DETECT
10586(A)
28
52
10176
29
41
10504
56
57
43
10503
31
10105
TO FRAME DETECTION & SYNCHRONIZATION BOARD #80
R
33
44
45

SYNC CIRCUIT)



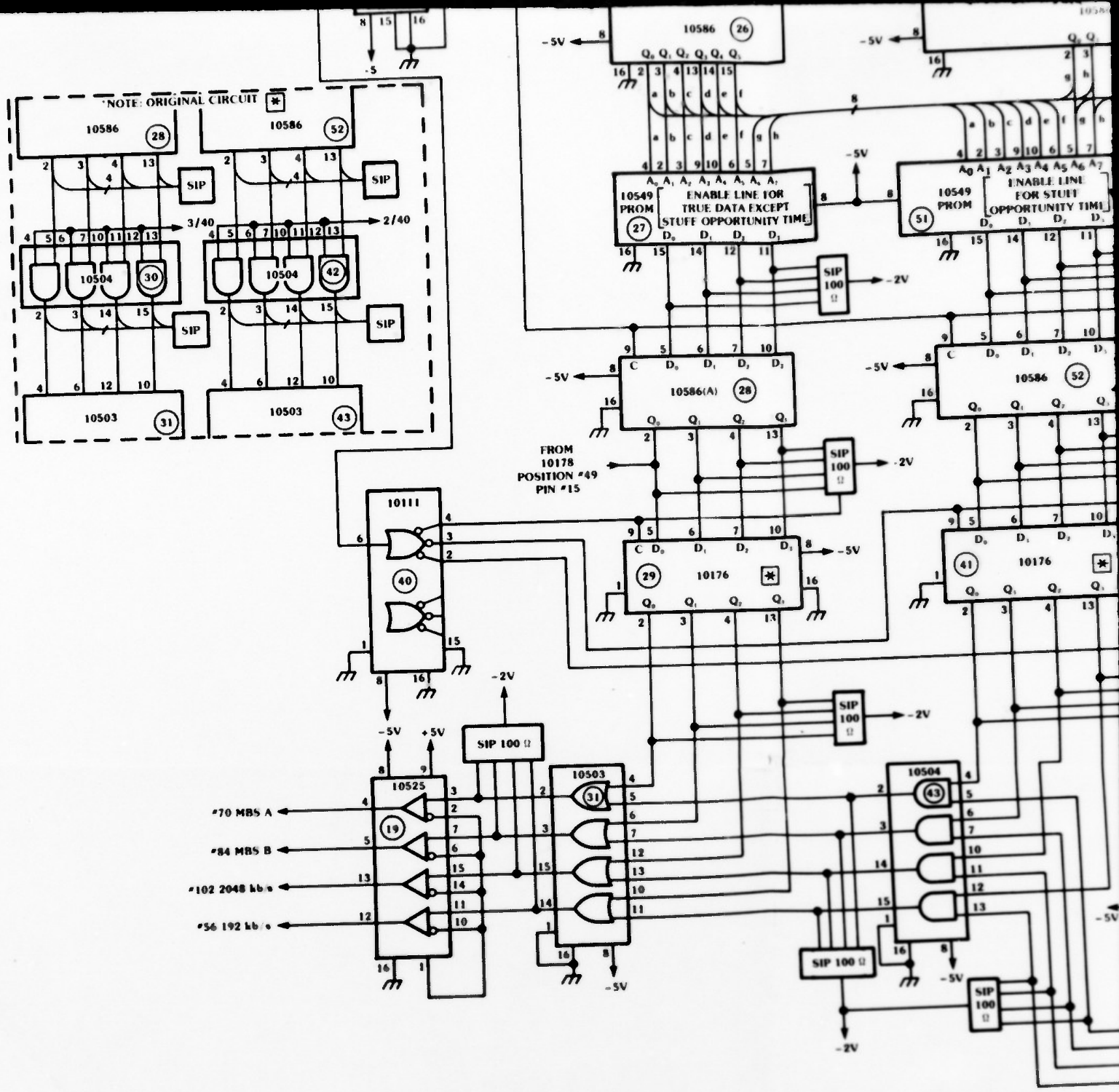

*NOTE: ORIGINAL CIRCUIT
10586 28
10586 52
SIP
3/40
2/40
10504 30
10504 42
10503 31
10503 43
10549 PROM 27
ENABLE LINE FOR TRUE DATA EXCEPT STUFF OPPORTUNITY TIME
10549 PROM 51
ENABLE LINE FOR STUFF OPPORTUNITY TIME
10586 26
10586(A) 28
10586 52
10111 40
10176 29
10176 41
FROM 10178 POSITION #49 PIN #15
SIP 100 Ω
-5V
-2V
+5V
10525 19
10503 31
10504 43
#70 MBS A
#84 MBS B
#102 2048 kb/s
#56 192 kb/s

Figure B-4. 3

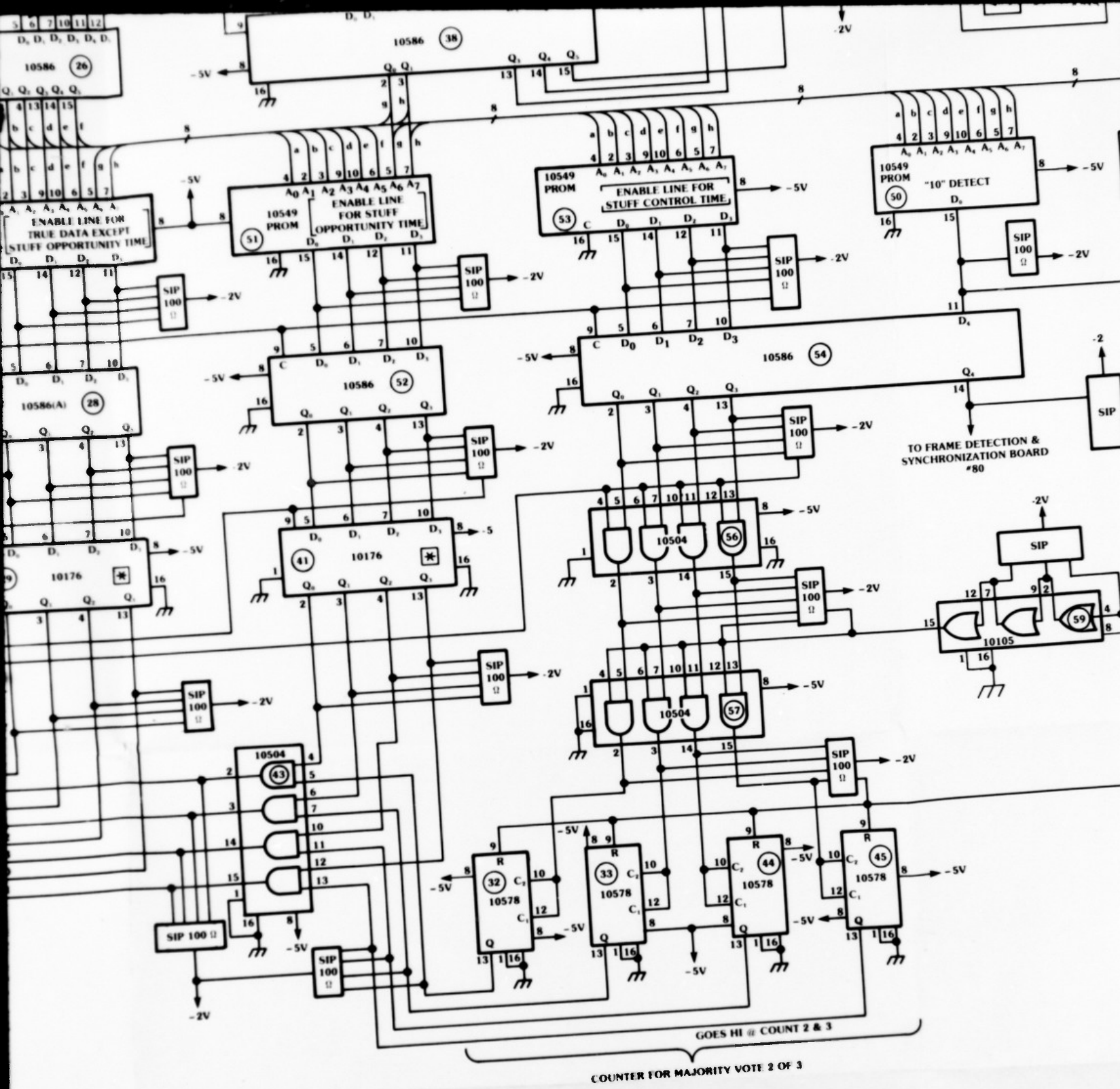
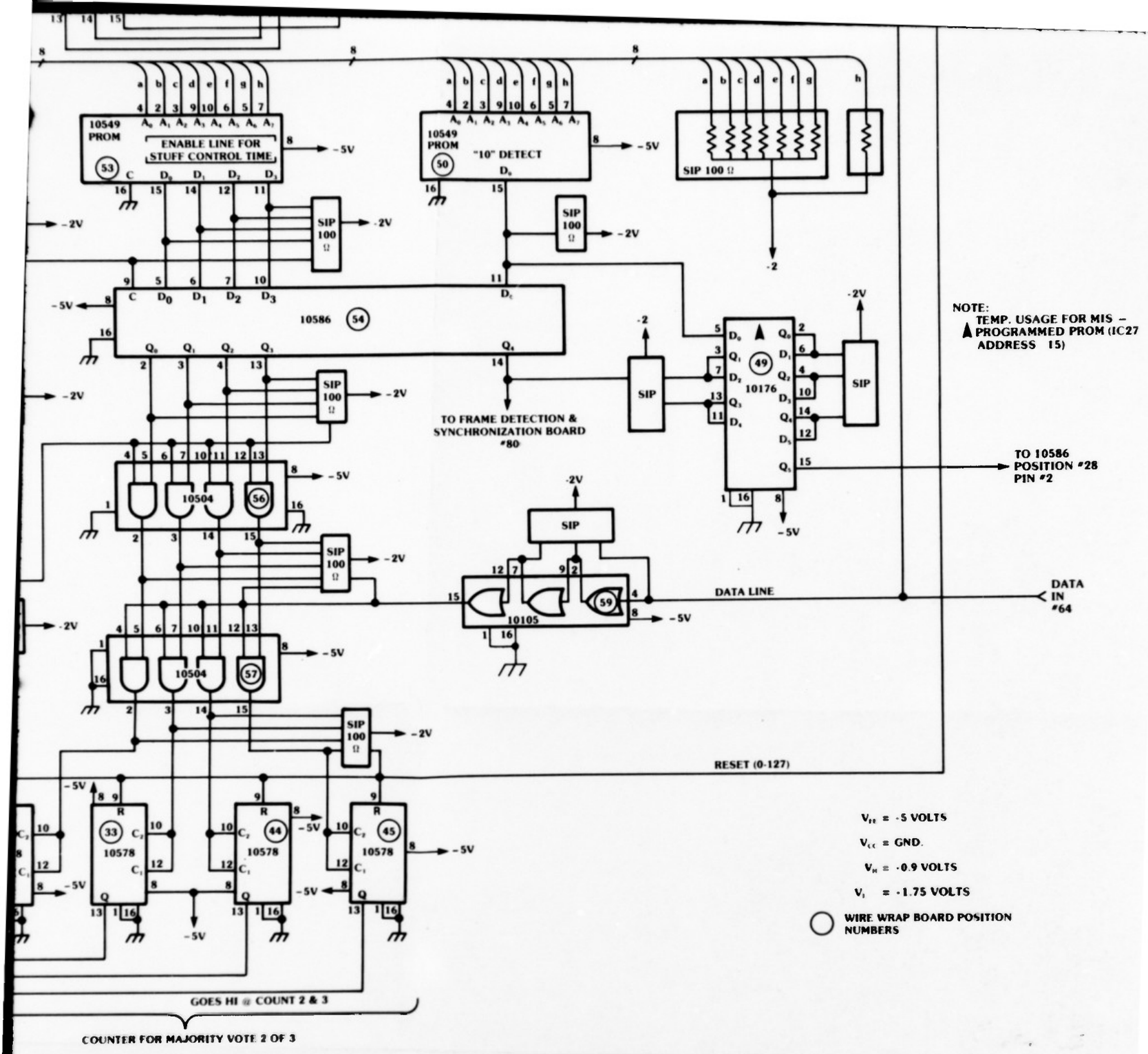
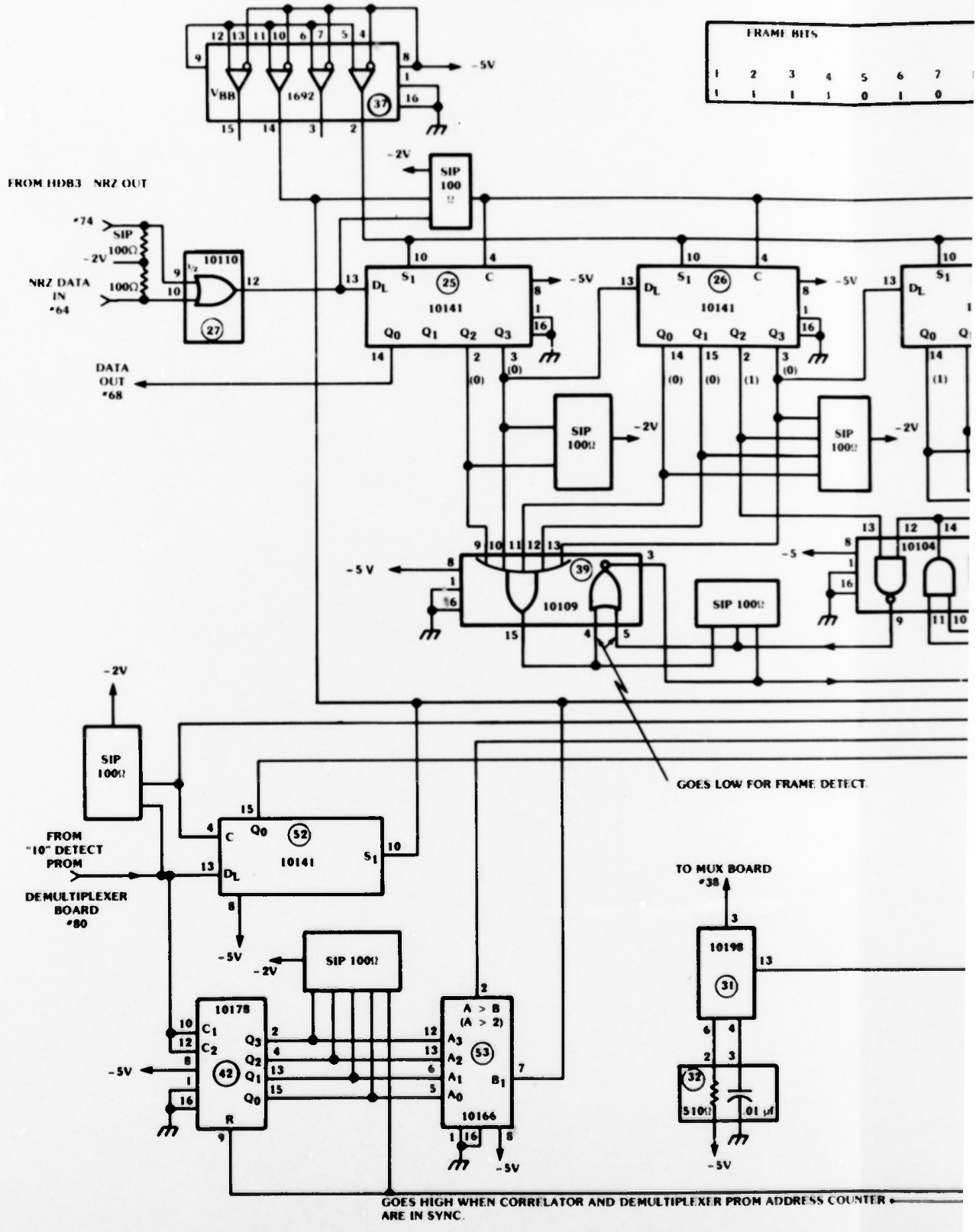


Figure B-4. 34 Mb/s DEMULTIPLEXER



DEMULTIPLEXER


FRAME BITS
1 2 3 4 5 6 7
1 1 1 1 0 1 0
FROM HDB3 NRZ OUT
NRZ DATA IN #64
DATA OUT #68
SIP 100Ω
SIP 100 Ω
-2V
-5V
10110
10141
10109
10104
1692
10178
10166
10198
A > B (A > 2)
GOES LOW FOR FRAME DETECT
FROM "10" DETECT PROM
DEMULTIPLEXER BOARD #80
TO MUX BOARD #38
510Ω
.01 μf
GOES HIGH WHEN CORRELATOR AND DEMULTIPLEXER PROM ADDRESS COUNTER ARE IN SYNC.

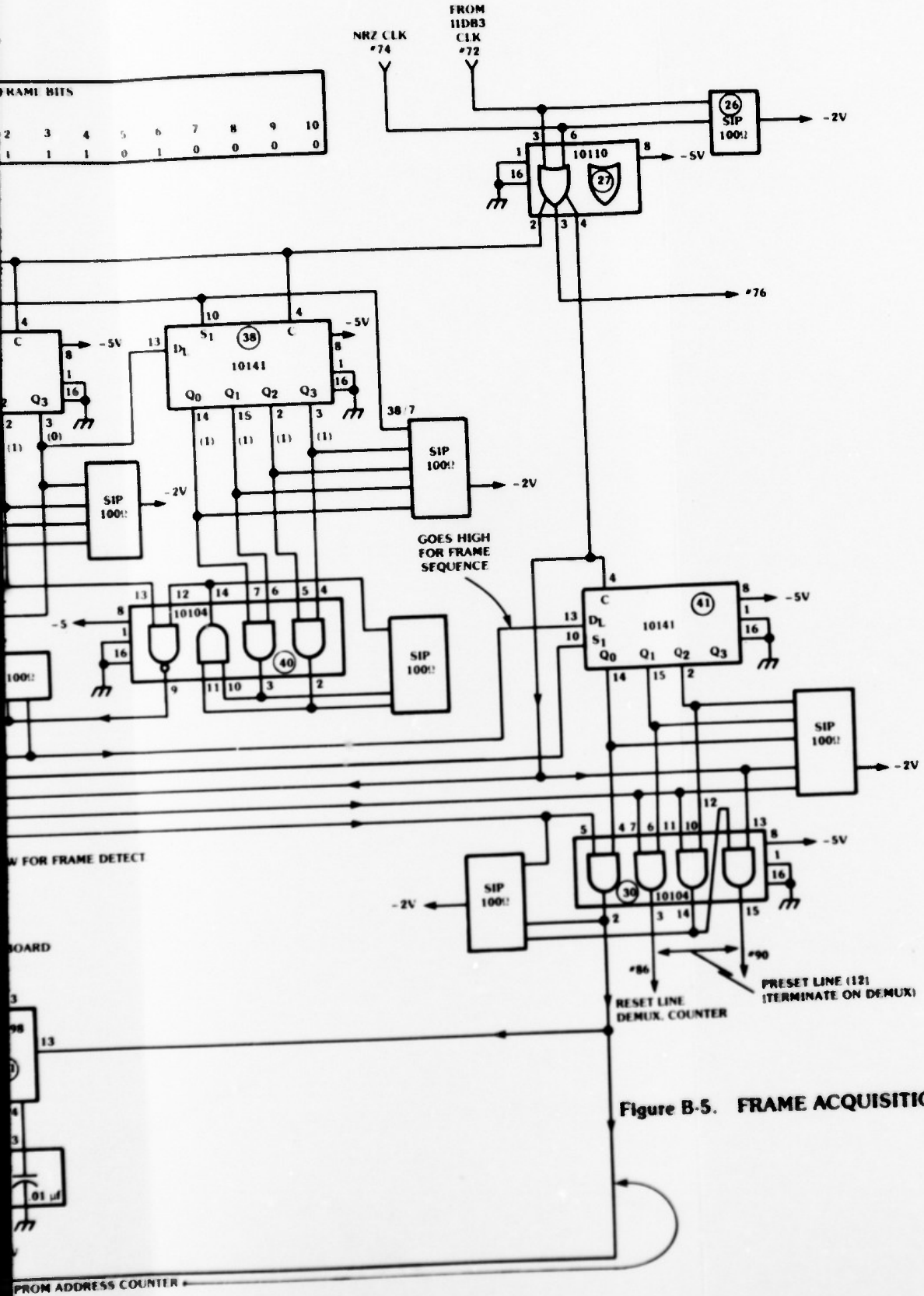
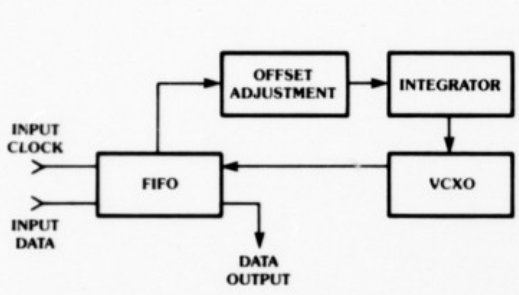
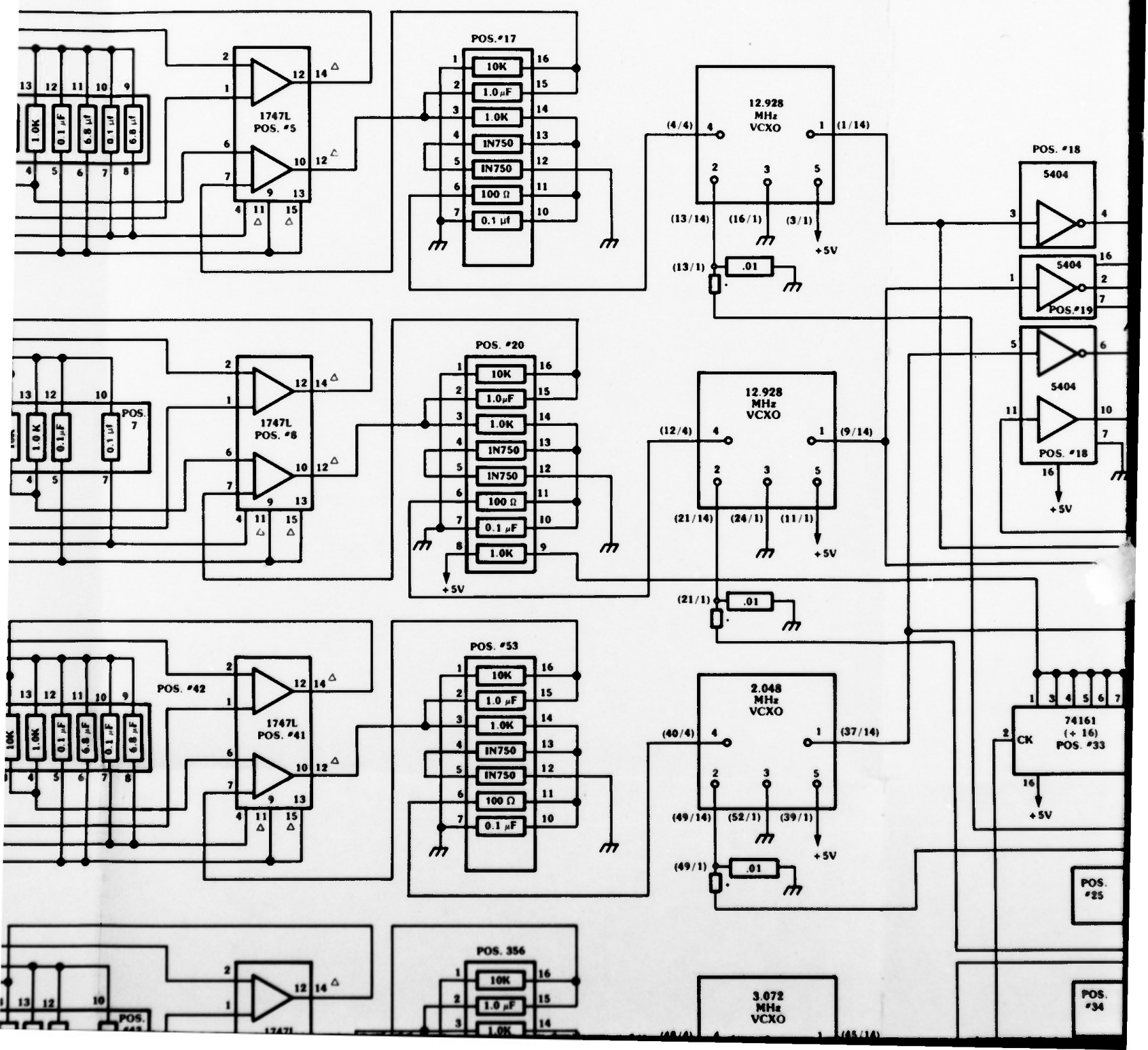
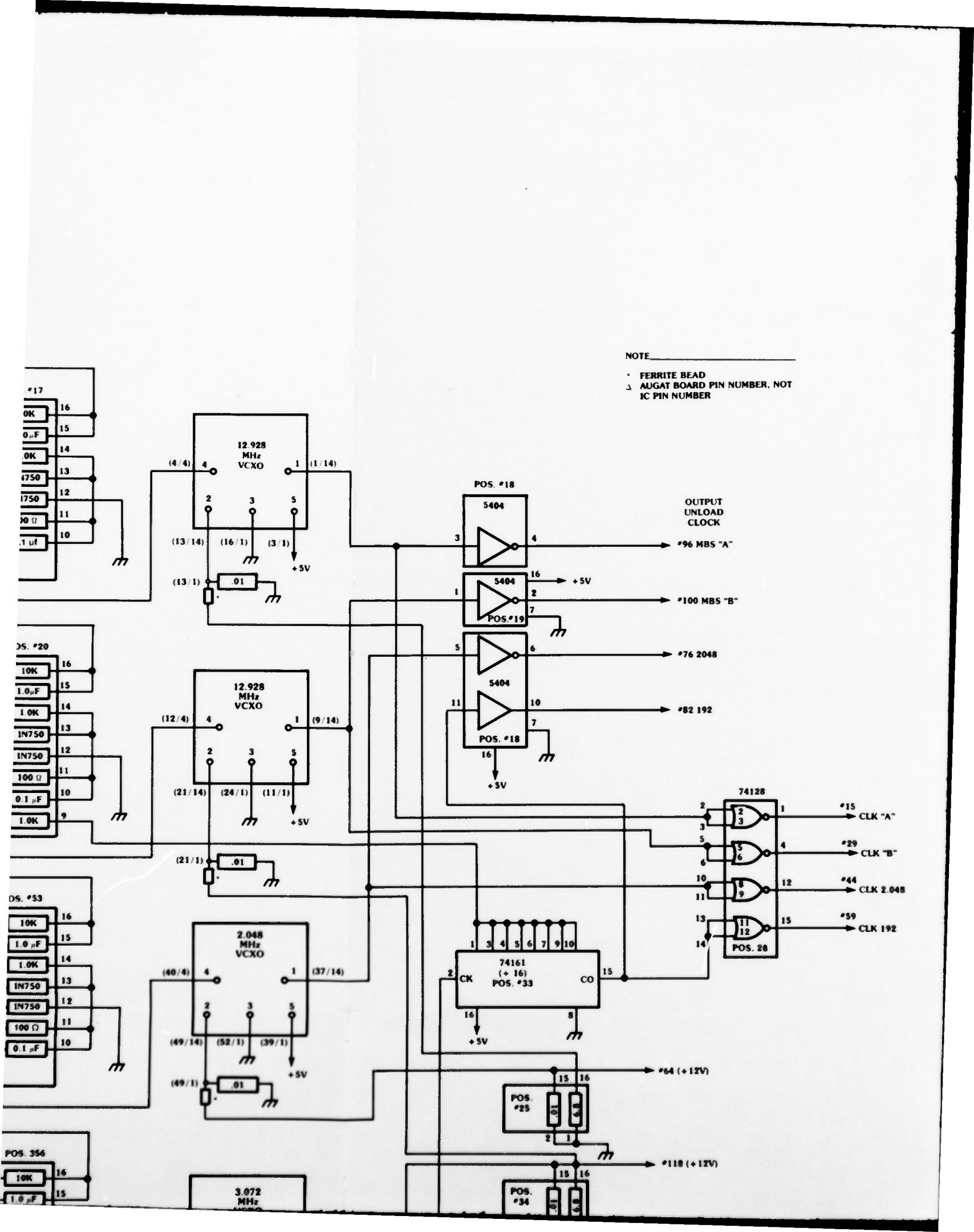


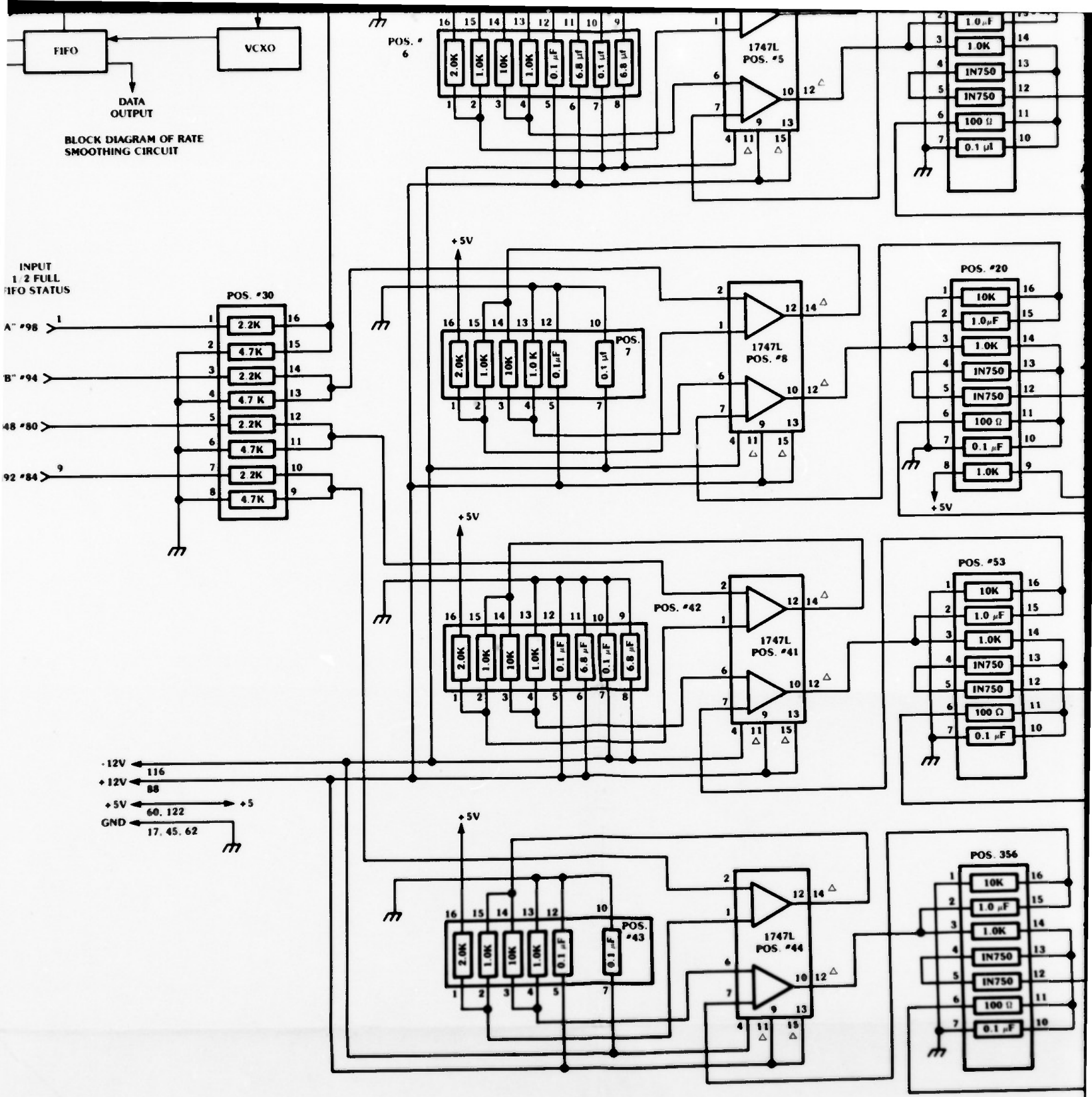
Figure B-5. FRAME ACQUISITION



BLOCK DIAGRAM OF RATE SMOOTHING CIRCUIT


1747L
POS. #5
POS.#17
10K
1.0 µF
1.0K
1N750
1N750
100 Ω
0.1 µf
12.928
MHz
VCXO
(4/4)
(1/14)
(13/14)
(16/1)
(3/1)
+5V
(13/1)
.01
POS. #18
5404
5404
POS.#19
5404
POS. #18
1747L
POS. #8
POS. #20
10K
1.0µF
1.0K
1N750
1N750
100 Ω
0.1 µF
1.0K
12.928
MHz
VCXO
(12/4)
(9/14)
(21/14)
(24/1)
(11/1)
+5V
(21/1)
.01
POS. #42
1747L
POS. #41
POS. #53
10K
1.0 µF
1.0K
1N750
1N750
100 Ω
0.1 µF
2.048
MHz
VCXO
(40/4)
(37/14)
(49/14)
(52/1)
(39/1)
+5V
(49/1)
.01
74161
(÷ 16)
POS. #33
CK
+5V
POS.
#25
POS. 356
10K
1.0 µF
1.0K
3.072
MHz
VCXO
POS.
#34


NOTE
• FERRITE BEAD
Δ AUGAT BOARD PIN NUMBER, NOT IC PIN NUMBER
12.928 MHz VCXO
(4/4)
(1/14)
(13/14)
(16/1)
(3/1)
+5V
(13/1)
.01
POS. #18
5404
OUTPUT UNLOAD CLOCK
#96 MBS "A"
#100 MBS "B"
POS. #19
#76 2048
#82 192
12.928 MHz VCXO
(12/4)
(9/14)
(21/14)
(24/1)
(11/1)
(21/1)
74128
#15 CLK "A"
#29 CLK "B"
#44 CLK 2.048
#59 CLK 192
POS. 28
2.048 MHz VCXO
(40/4)
(37/14)
(49/14)
(52/1)
(39/1)
(49/1)
74161 (÷ 16) POS. #33
CK
CO
#64 (+12V)
POS. #25
#118 (+12V)
POS. #34
POS. 356
3.072 MHz


FIFO
VCXO
DATA OUTPUT
BLOCK DIAGRAM OF RATE SMOOTHING CIRCUIT
INPUT 1/2 FULL FIFO STATUS
POS. #30
2.2K
4.7K
4.7K
2.2K
4.7K
2.2K
4.7K
+5V
1747L POS. #5
1747L POS. #8
1747L POS. #41
1747L POS. #44
POS. #20
POS. #53
POS. 356
10K
1.0 µF
1.0K
IN750
100 Ω
0.1 µF
-12V
+12V
+5V
GND
116
88
60. 122
17. 45. 62

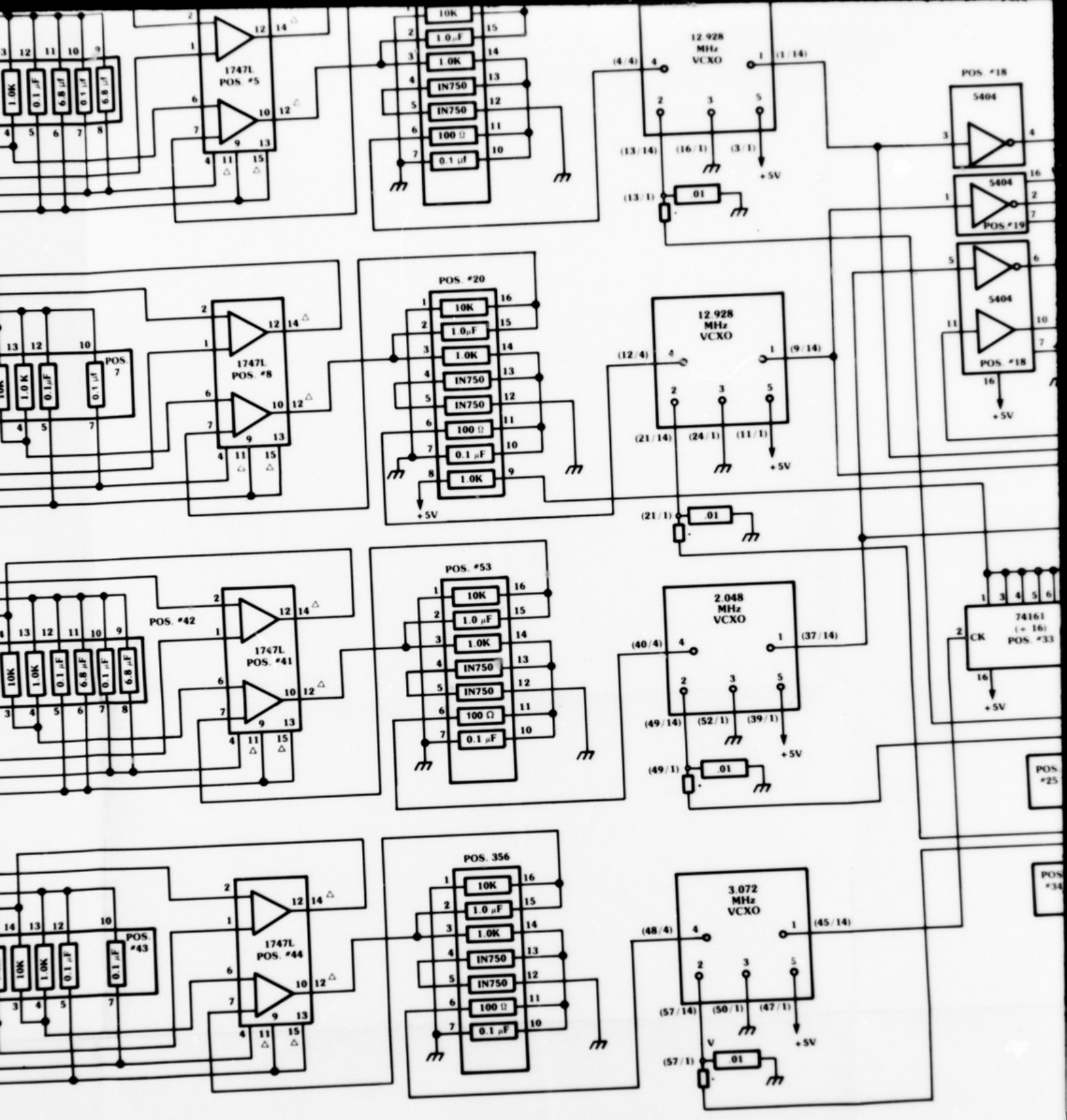


Figure B-6. RATE SMOOTHING

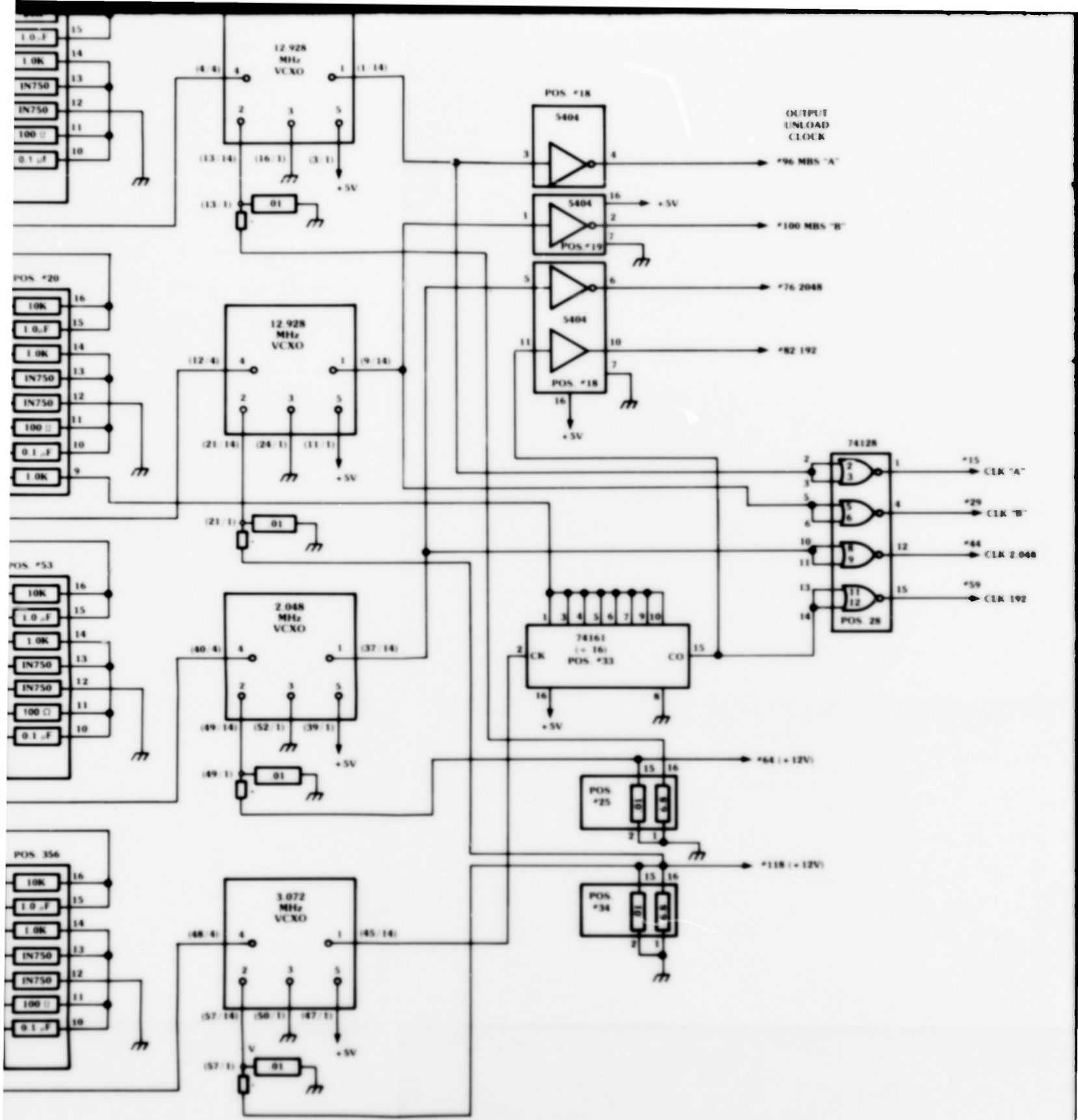
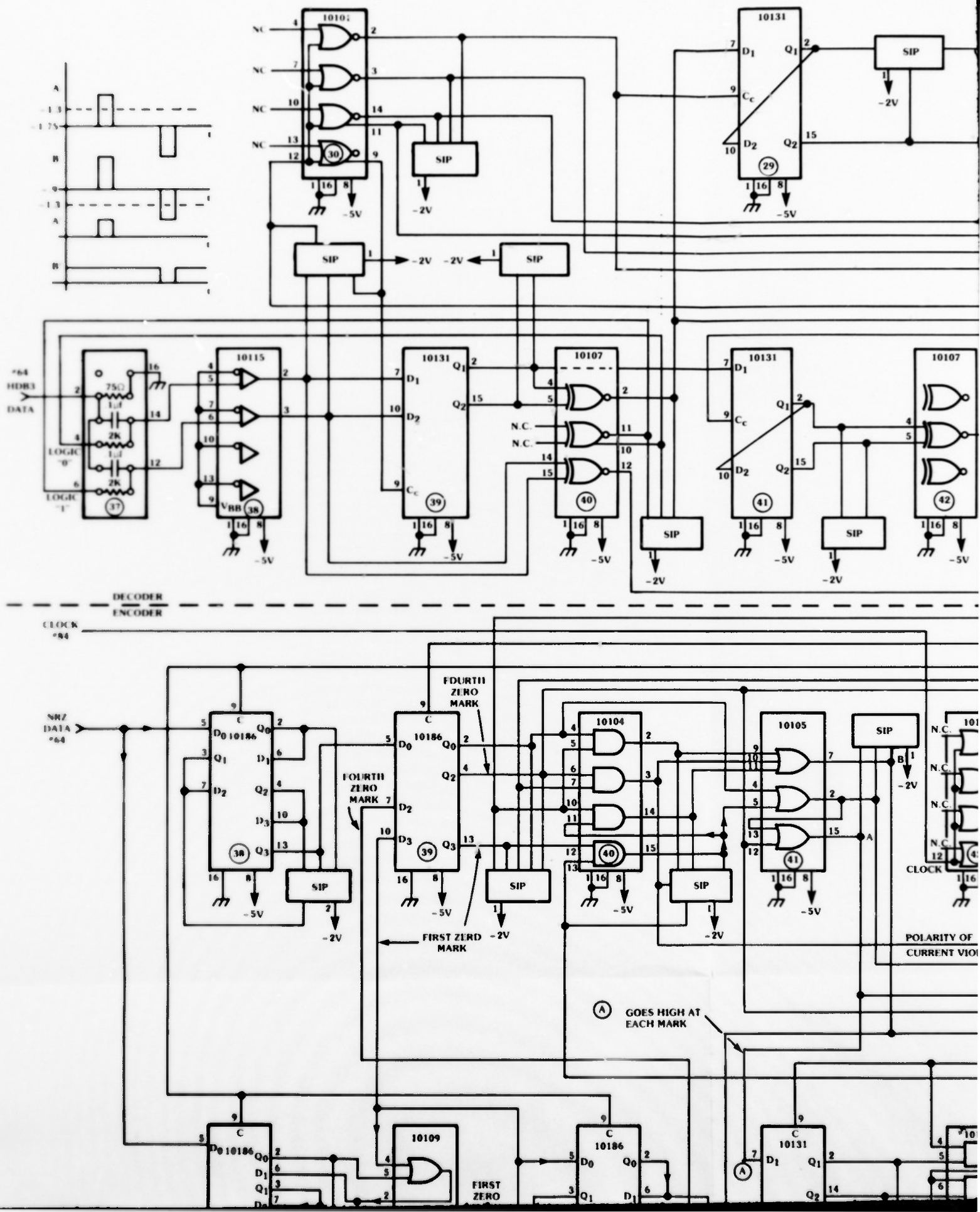
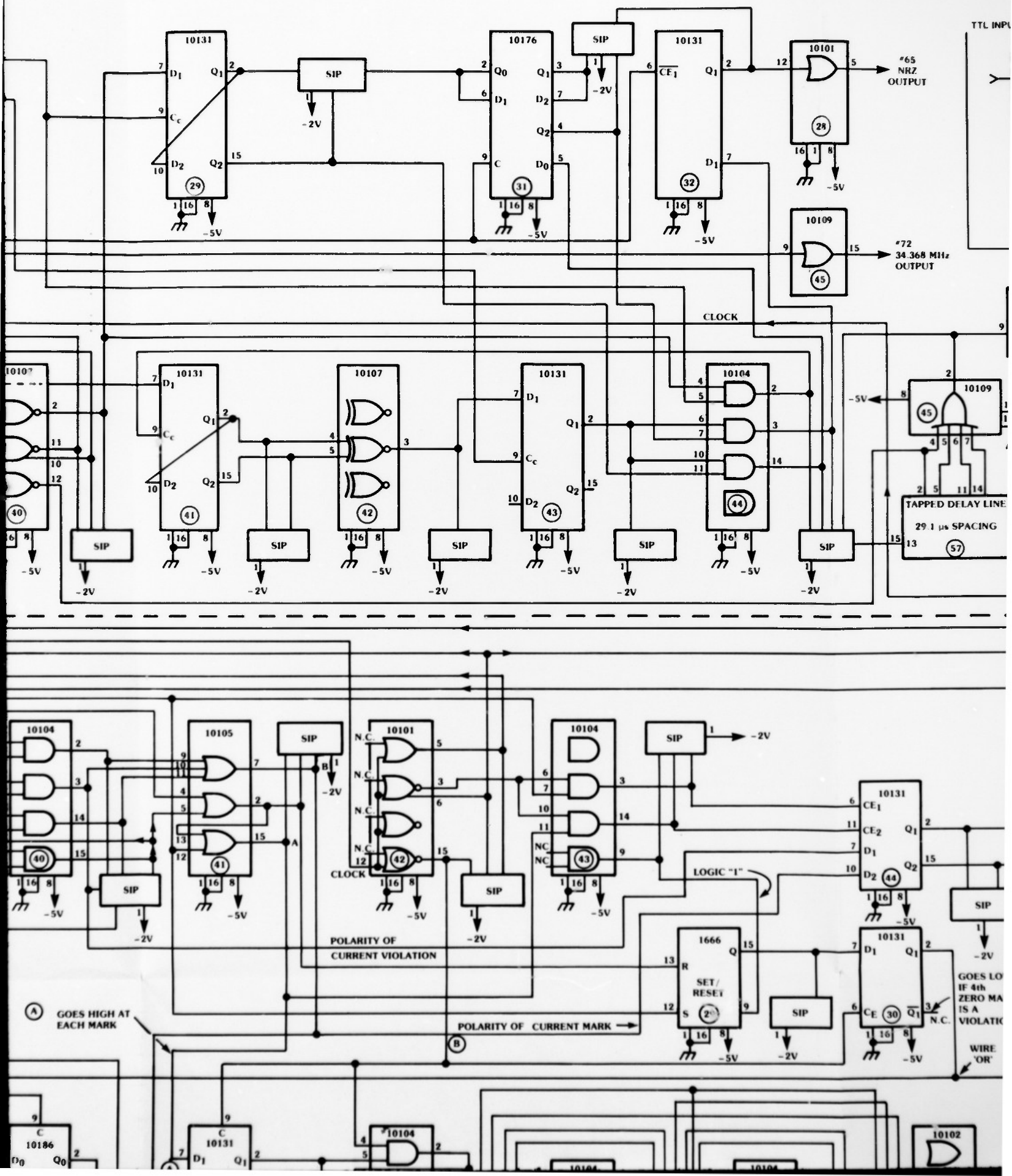
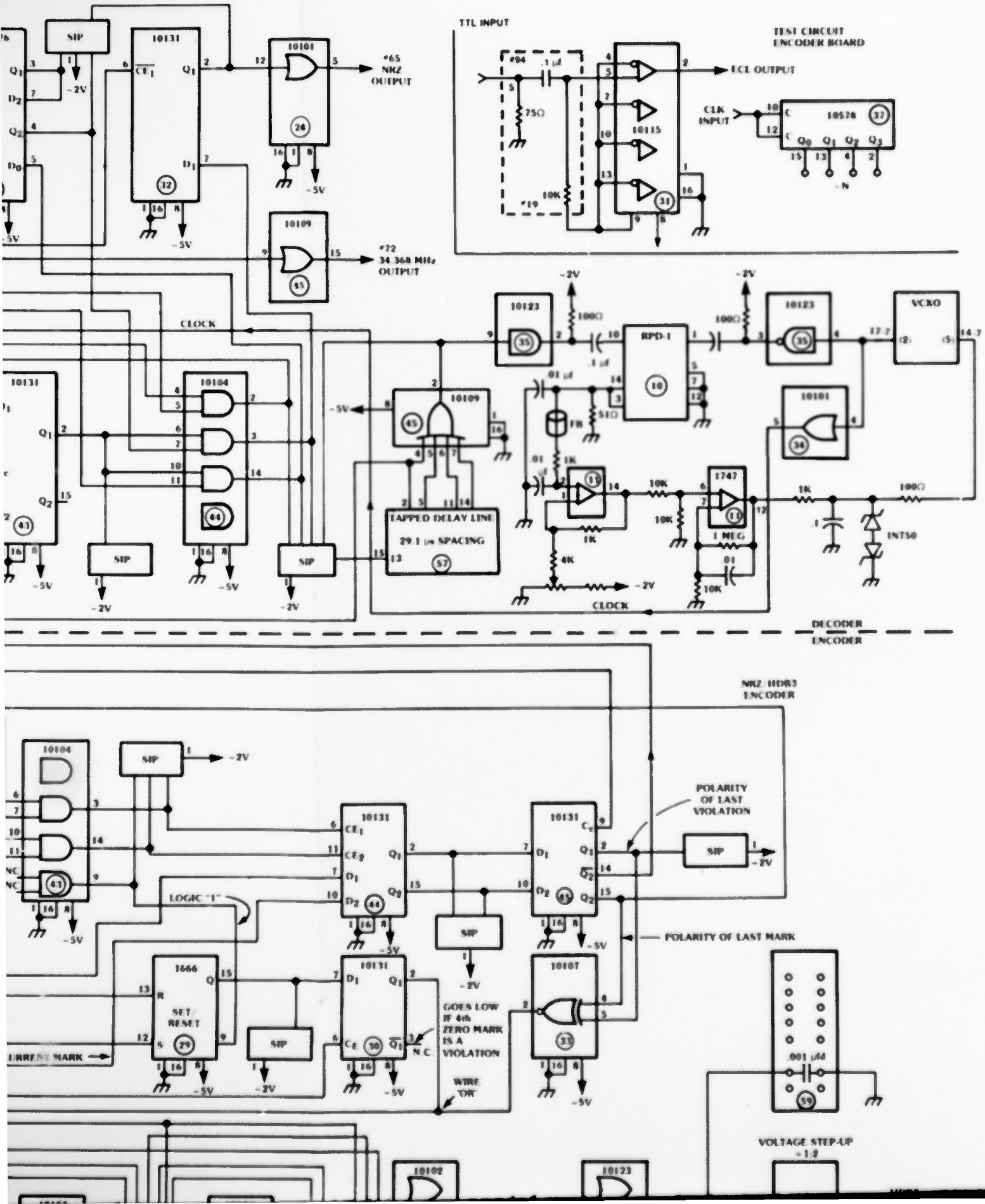
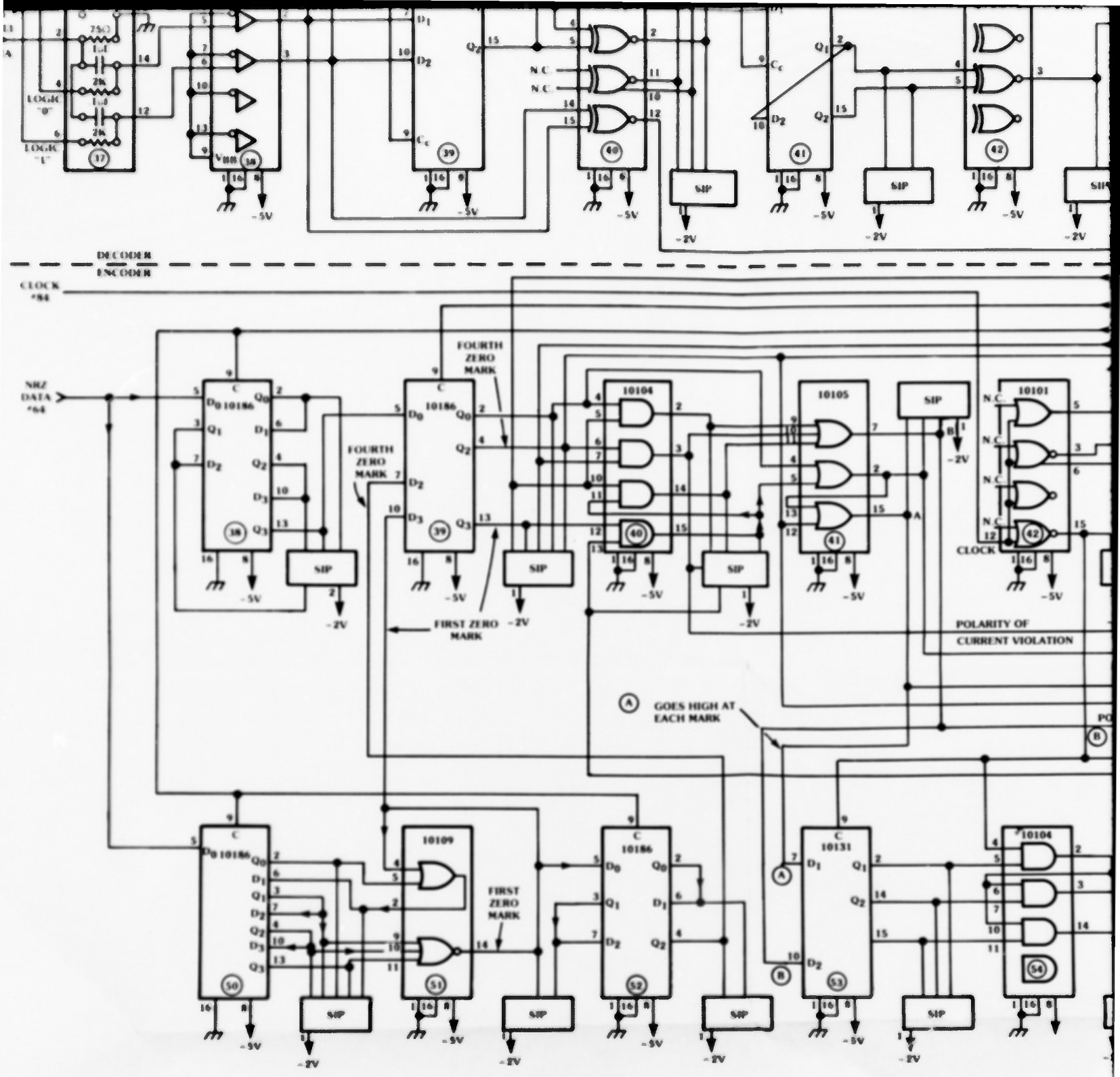


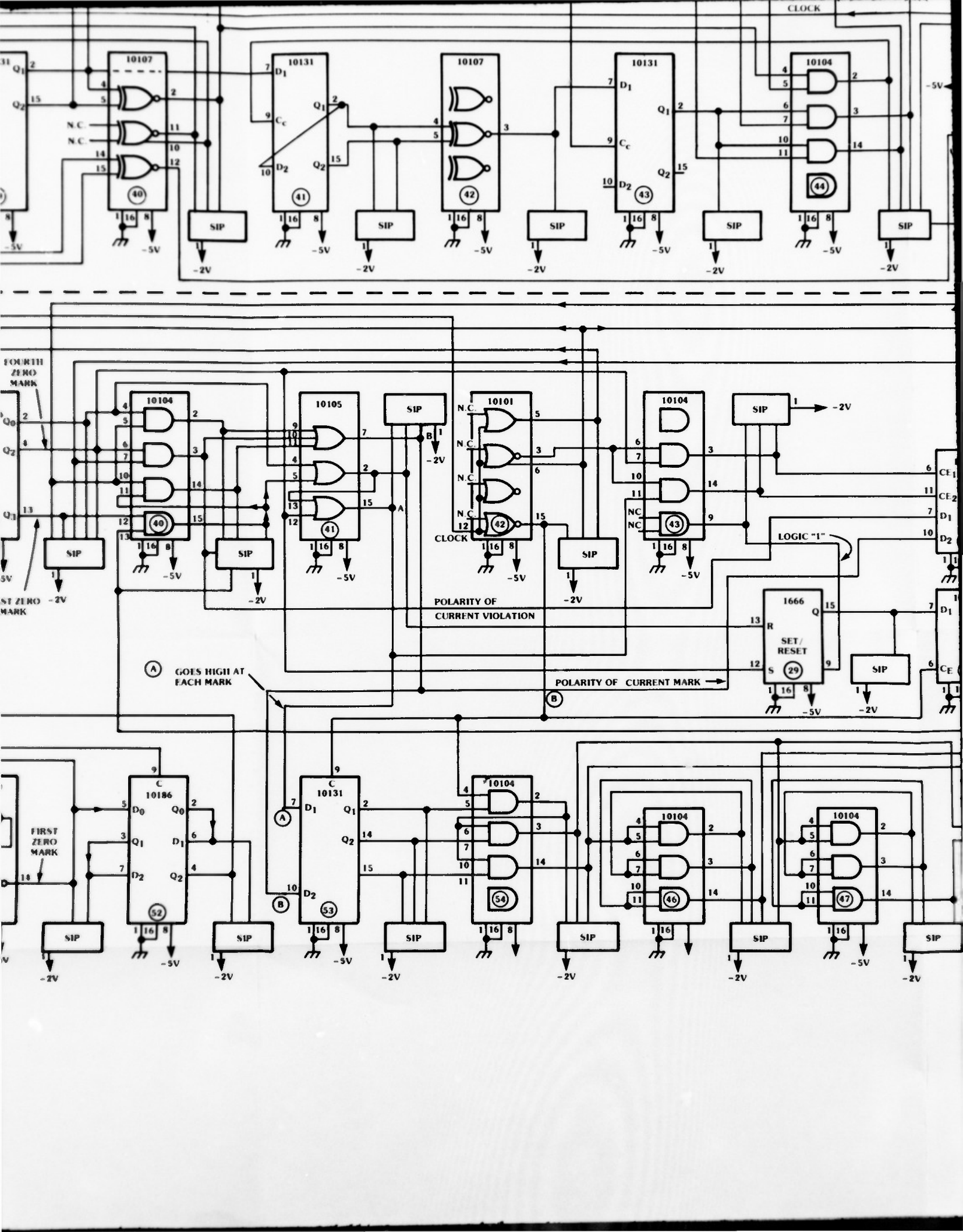
Figure B-6. RATE SMOOTHING


10101
10131
SIP
-2V
-5V
10115
10107
75Ω
1μf
2K
*64
HDB3
DATA
LOGIC "0"
LOGIC "1"
N.C.
DECODER
ENCODER
CLOCK *64
NRZ DATA *64
10186
10104
10105
10109
FOURTH ZERO MARK
FIRST ZERO MARK
POLARITY OF
GOES HIGH AT EACH MARK
FIRST ZERO


10131
10176
SIP
10101
#65
NRZ
OUTPUT
10109
#72
34.368 MHz
OUTPUT
CLOCK
10107
10104
TAPPED DELAY LINE
29.1 μs SPACING
10105
10186
1666
SET/
RESET
LOGIC "1"
POLARITY OF
CURRENT VIOLATION
POLARITY OF CURRENT MARK
GOES HIGH AT
EACH MARK
GOES LO
IF 4th
ZERO MA
IS A
VIOLATIO
WIRE
'OR'
N.C.
-5V
-2V


TTL INPUT
TEST CIRCUIT
ENCODER BOARD
ECL OUTPUT
CLK INPUT
*65
NRZ
OUTPUT
*72
34.368 MHz
OUTPUT
CLOCK
TAPPED DELAY LINE
29.1 ns SPACING
VCXO
INTSO
DECODER
ENCODER
NRZ HDB3
ENCODER
POLARITY
OF LAST
VIOLATION
LOGIC "1"
POLARITY OF LAST MARK
SET
RESET
GOES LOW
IF 4th
ZERO MARK
IS A
VIOLATION
WIRE
"OR"
VOLTAGE STEP-UP
-1.9


DECODER
ENCODER
CLOCK
*64
NRZ
DATA
*64
FOURTH
ZERO
MARK
FIRST ZERO
MARK
10186
10104
10105
10101
10109
10131
SIP
-5V
-2V
POLARITY OF
CURRENT VIOLATION
GOES HIGH AT
EACH MARK
CLOCK


CLOCK
10107
10131
10104
SIP
-5V
-2V
FOURTH ZERO MARK
FIRST ZERO MARK
10105
10101
10186
10131
1666
SET/ RESET
LOGIC "1"
POLARITY OF CURRENT VIOLATION
POLARITY OF CURRENT MARK
A GOES HIGH AT EACH MARK
N.C.
NC

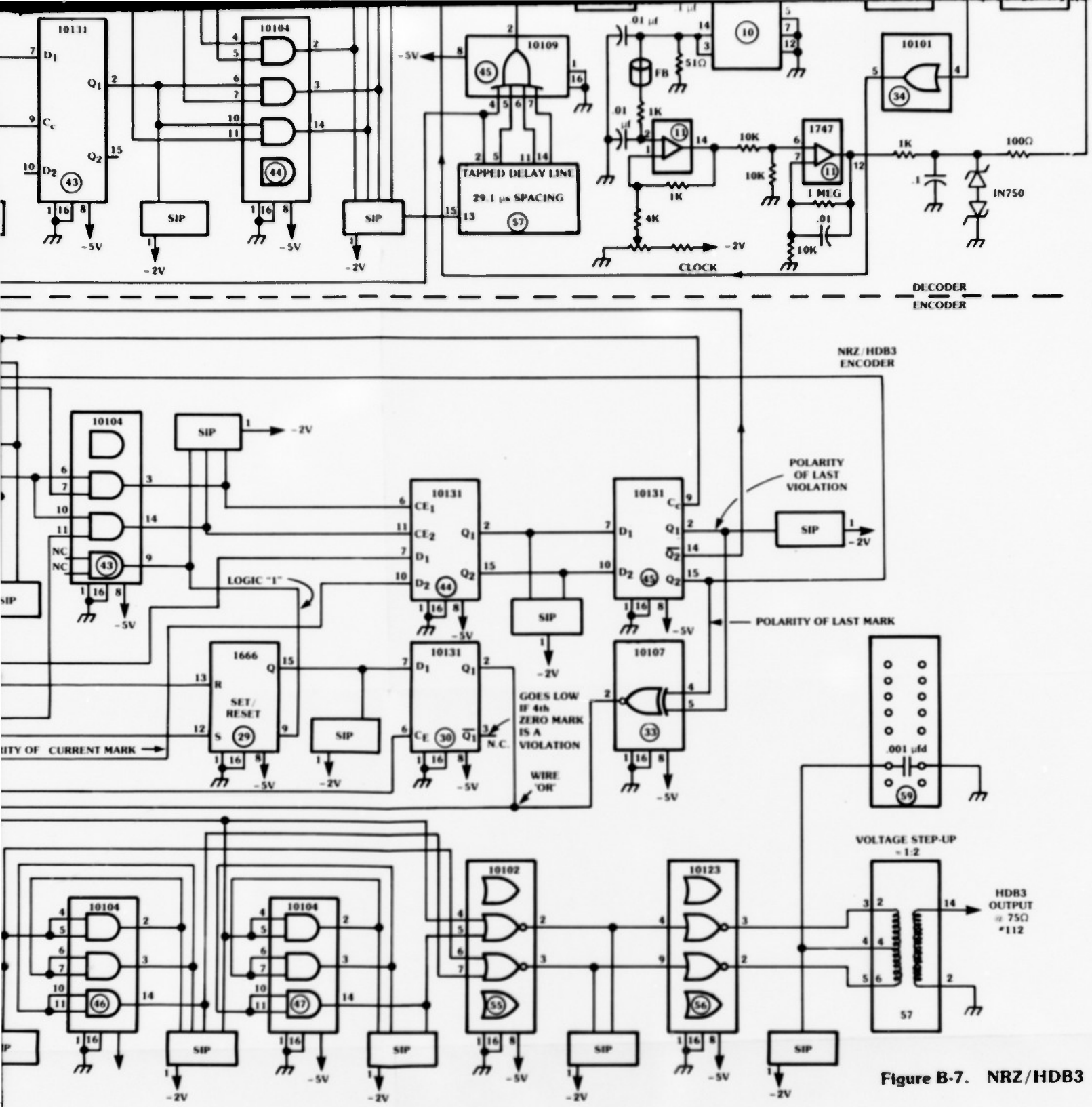
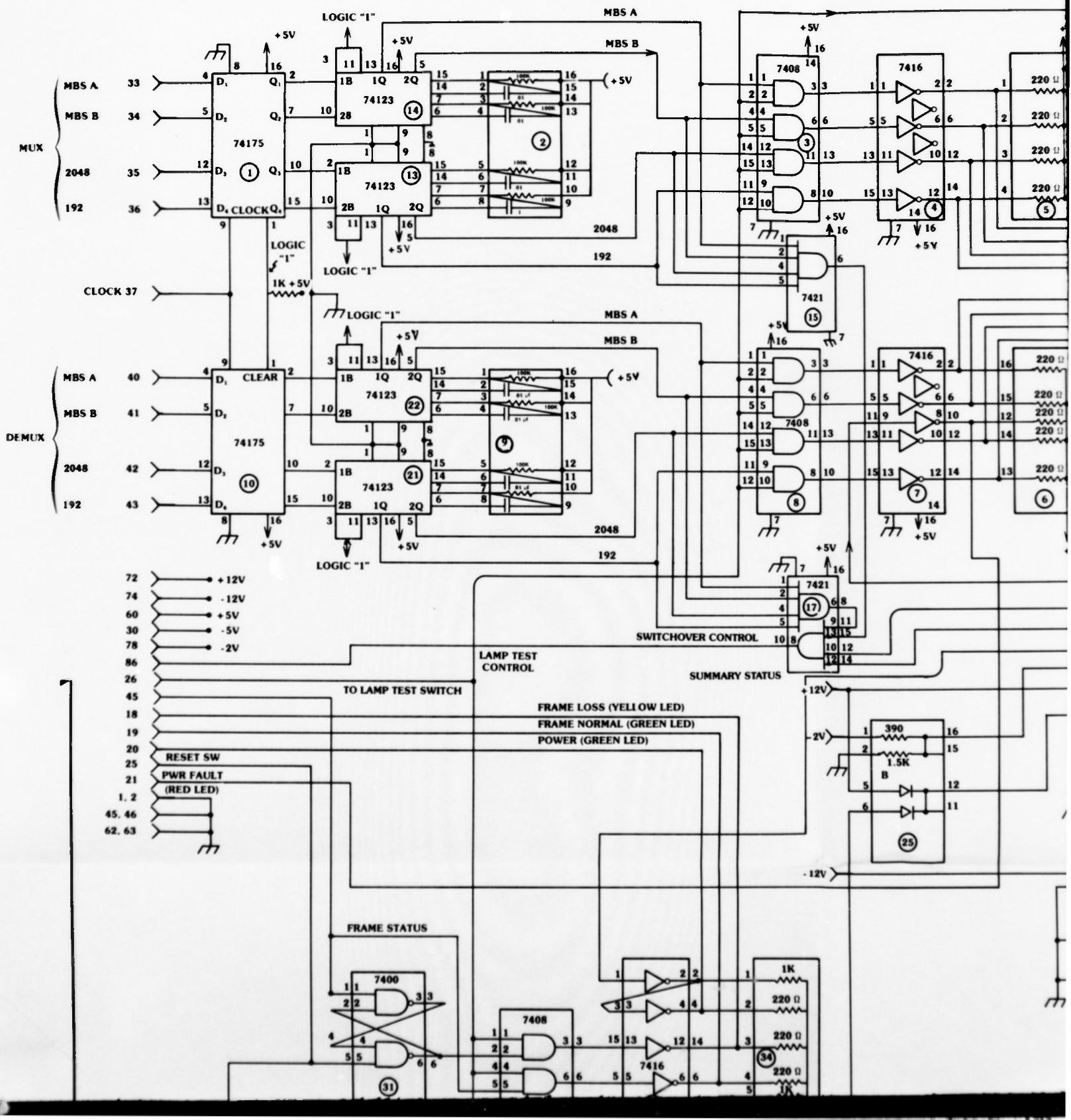
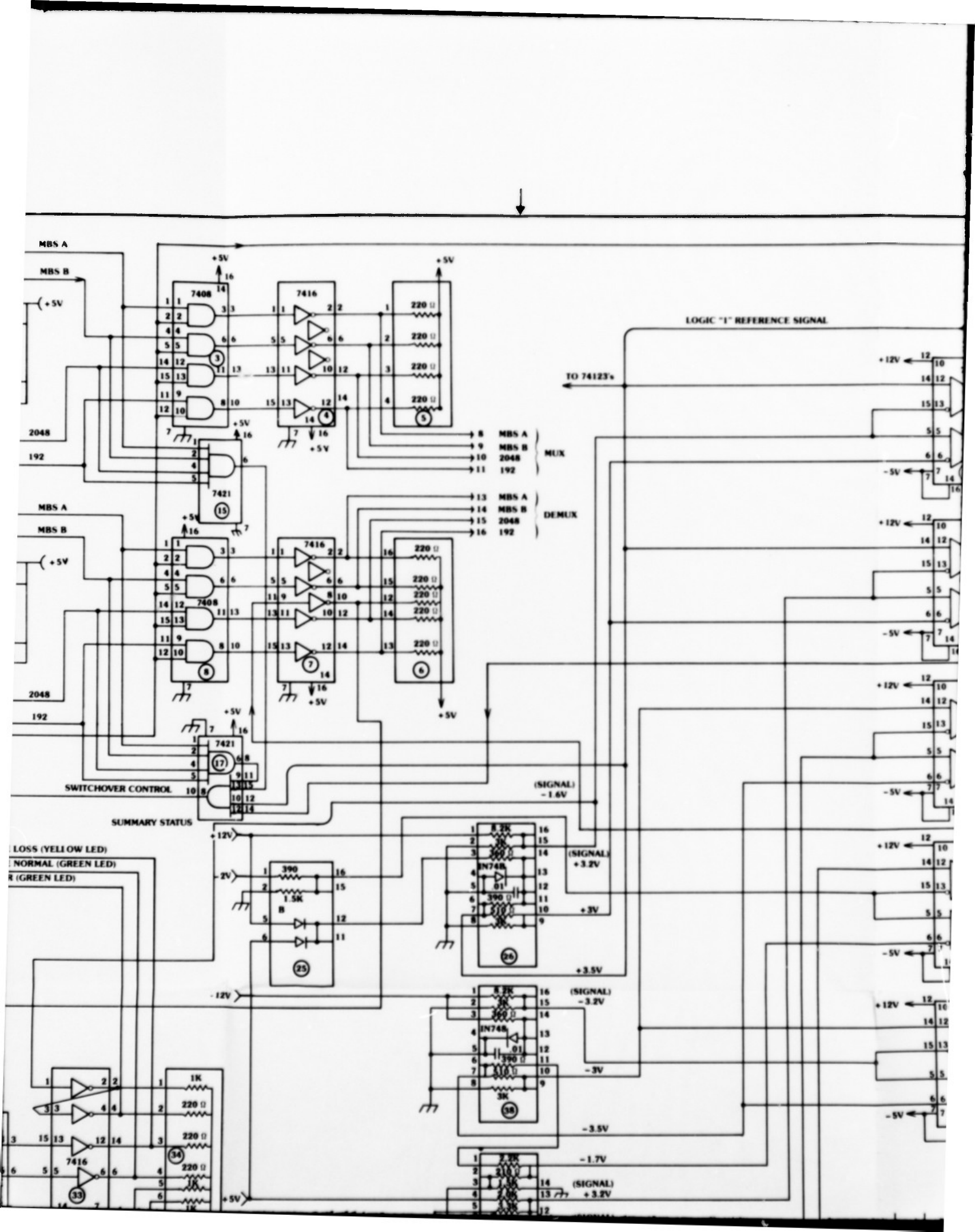
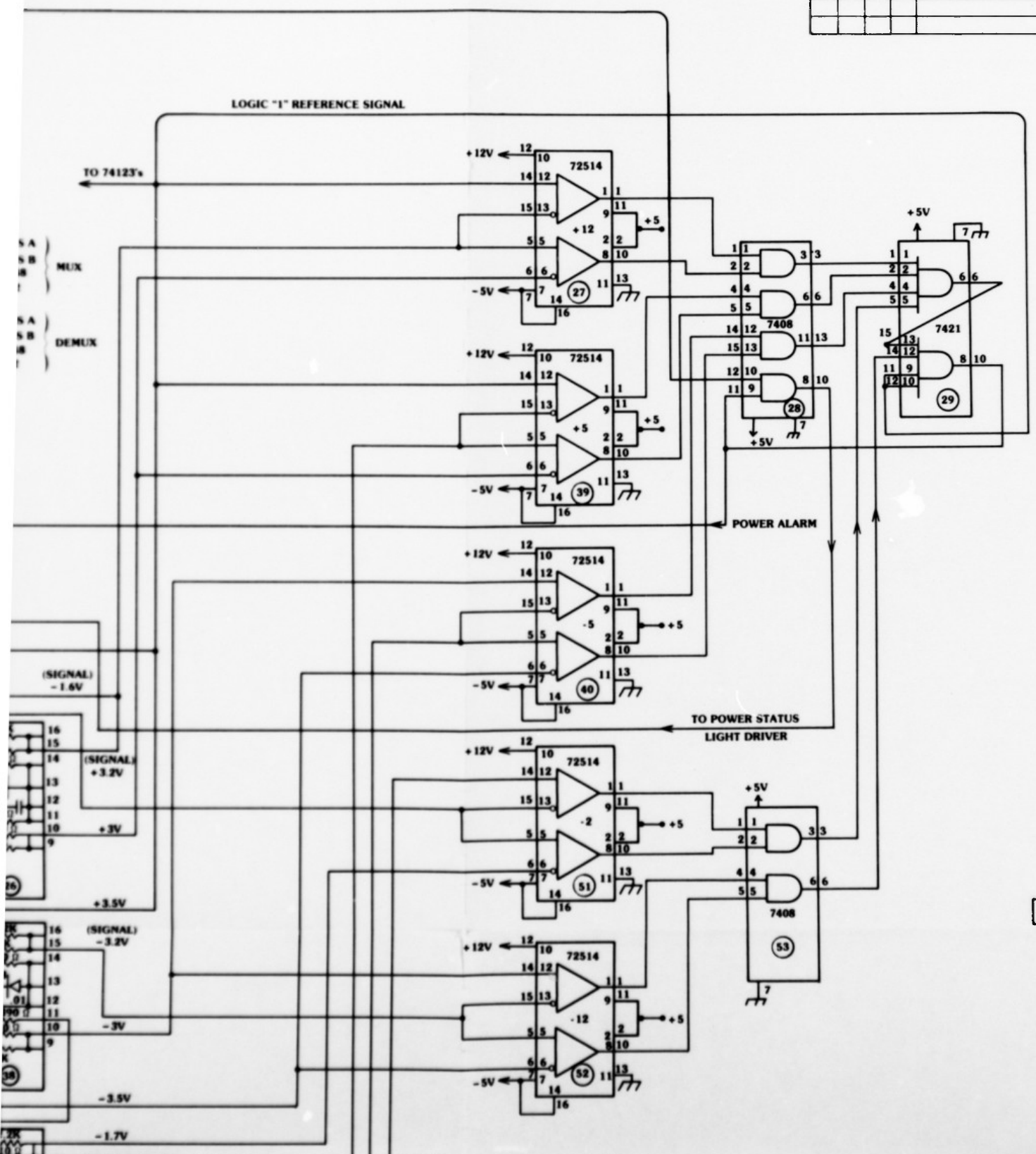


Figure B-7. NRZ/HDB3

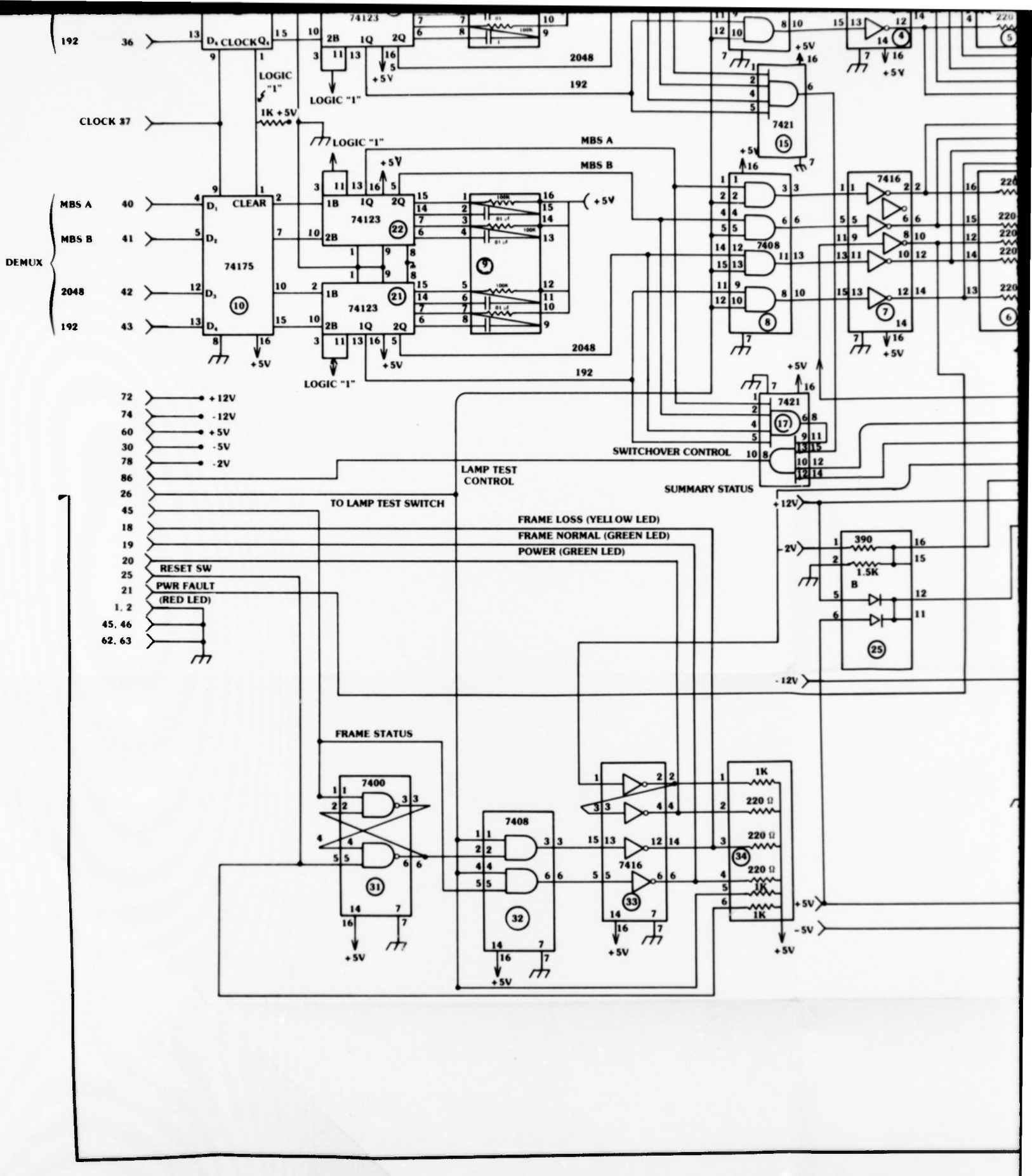

MUX
MBS A
MBS B
2048
192
CLOCK 37
74175
74123
7408
7416
7421
7400
LOGIC "1"
+5V
1K
220 Ω
390
1.5K
DEMUX
CLEAR
CLOCK
+12V
-12V
-5V
-2V
LAMP TEST CONTROL
TO LAMP TEST SWITCH
SWITCHOVER CONTROL
SUMMARY STATUS
FRAME LOSS (YELLOW LED)
FRAME NORMAL (GREEN LED)
POWER (GREEN LED)
RESET SW
PWR FAULT
(RED LED)
FRAME STATUS


MBS A
MBS B
+5V
7408
7416
7421
220 Ω
LOGIC "1" REFERENCE SIGNAL
TO 74123's
2048
192
MUX
DEMUX
SWITCHOVER CONTROL
SUMMARY STATUS
(SIGNAL) -1.6V
(SIGNAL) +3.2V
(SIGNAL) -3.2V
(SIGNAL) +3.2V
+12V
-12V
+2V
+3V
-3V
+3.5V
-3.5V
-1.7V
-5V
390
1.5K
1K
3K
8.2K
IN748
LOSS (YELLOW LED)
NORMAL (GREEN LED)
(GREEN LED)

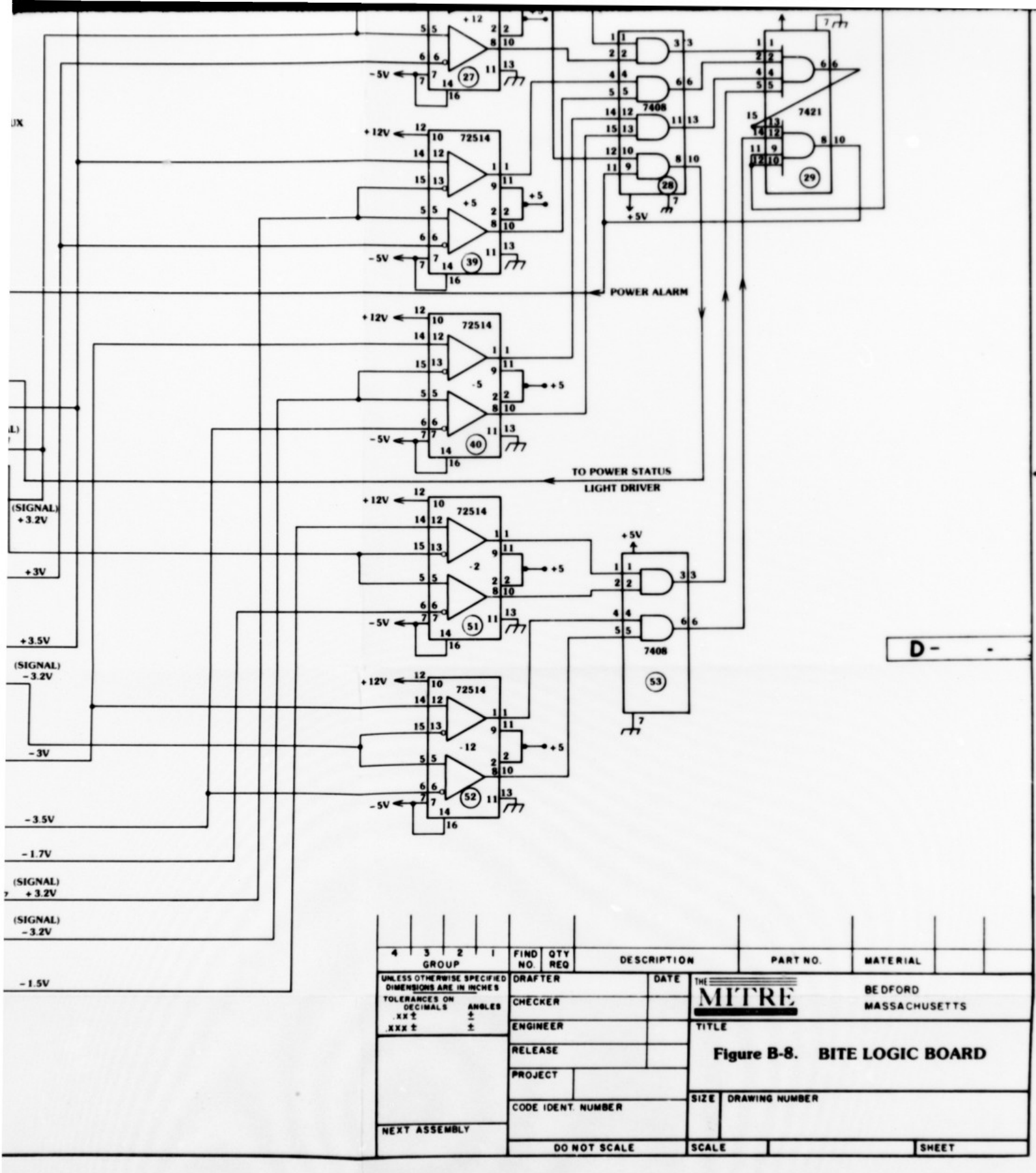
CHANGE LETTER	DRN BY	CHK'D BY	DATE	CHANGES



D- -


192
36
CLOCK 37
LOGIC "1"
1K +5V
MBS A
40
MBS B
41
DEMUX
2048
42
192
43
74175
74123
74123
74123
CLEAR
LOGIC "1"
LOGIC "1"
+5V
MBS A
MBS B
2048
192
2048
192
7421
7408
7416
7400
72 +12V
74 -12V
60 +5V
30 -5V
78 -2V
86
26
45
18
19
20
25
21
1, 2
45, 46
62, 63
LAMP TEST CONTROL
TO LAMP TEST SWITCH
SWITCHOVER CONTROL
SUMMARY STATUS
FRAME LOSS (YELLOW LED)
FRAME NORMAL (GREEN LED)
POWER (GREEN LED)
RESET SW
PWR FAULT
(RED LED)
FRAME STATUS
390
1.5K
220 Ω
1K
+12V
-12V
-2V
-5V

8 MBS A
9 MBS B
10 2048
11 192
MUX
13 MBS A
14 MBS B
15 2048
16 192
DEMUX
7421
7416
7408
220 Ω
+5V
SWITCHOVER CONTROL
SUMMARY STATUS
(SIGNAL) -1.6V
(SIGNAL) +3.2V
(SIGNAL) -3.2V
(SIGNAL) +3.2V
(SIGNAL) -3.2V
+12V
-12V
+3V
+3.5V
-3V
-3.5V
-1.7V
-1.5V
8.2K
3K
360 Ω
390 Ω
510 Ω
1.5K
1K
2.2K
2.7K
1.8K
3.3K
IN748
.01
B
S (YELLOW LED)
IMAL (GREEN LED)
EEN LED)
UNLESS OTHERW
DIMENSIONS A
TOLERANCES
DECIMAL
.XX ±
.XXX ±
NEXT ASSE



D- -

4 3 2 1 GROUP	FIND NO.	QTY REQ	DESCRIPTION	PART NO.	MATERIAL	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS: .XX ± .XXX ± ANGLES ±	DRAFTER		DATE	THE MITRE	BEDFORD MASSACHUSETTS	
	CHECKER					
	ENGINEER			TITLE		
	RELEASE			**Figure B-8. BITE LOGIC BOARD**		
	PROJECT					
	CODE IDENT. NUMBER			SIZE	DRAWING NUMBER	
NEXT ASSEMBLY	DO NOT SCALE			SCALE		SHEET

ADAPTER BOARD

XTAL PIN #	SOCKET POSITION #	BOARD EDGE PIN #
1 GND & RF RET	50	1
2 CASE	51	1
3 B+	52	3
4 RF OUT	38	4

XTAL PIN #	SOCKET POSITION #	BOARD EDGE PIN #
1 GND & RF RET	22	1
2 CASE	23	1
3 B+	24	3
4 RF OUT	11	4

XTAL PIN #	SOCKET POSITION #	BOARD EDGE PIN #
1 0V & RF RET	14	1
2 CASE	15	1
3 B+	16	3
4 RF OUT	3	4

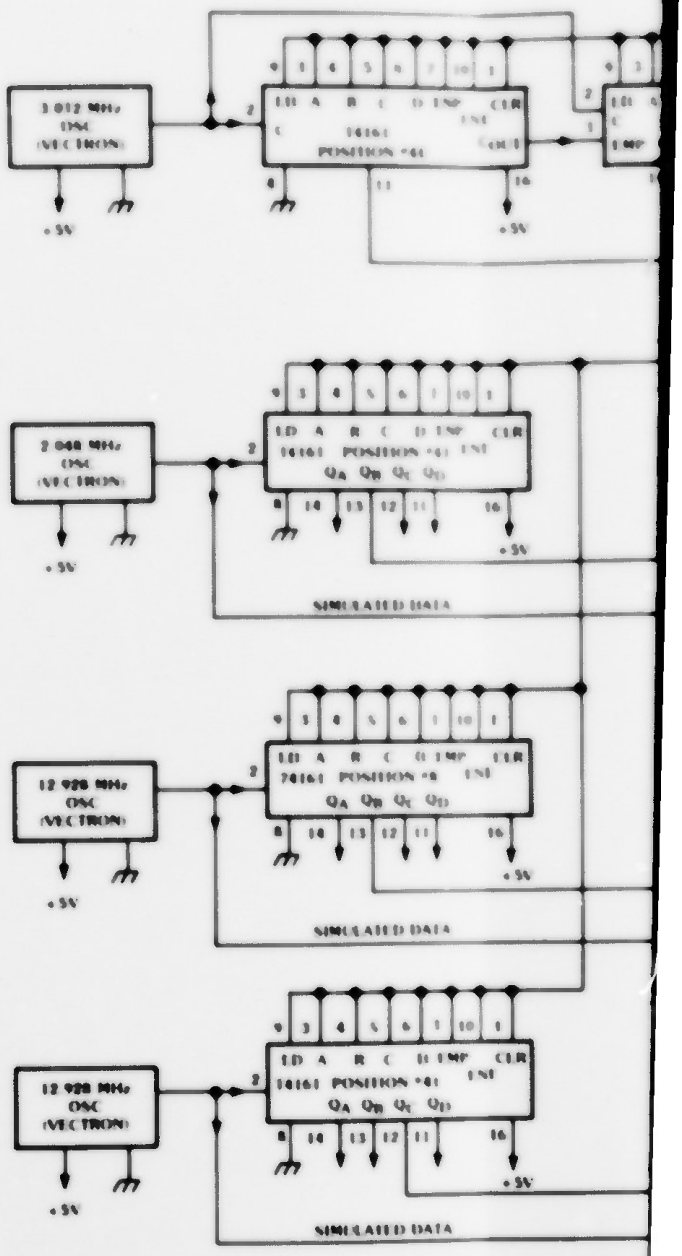
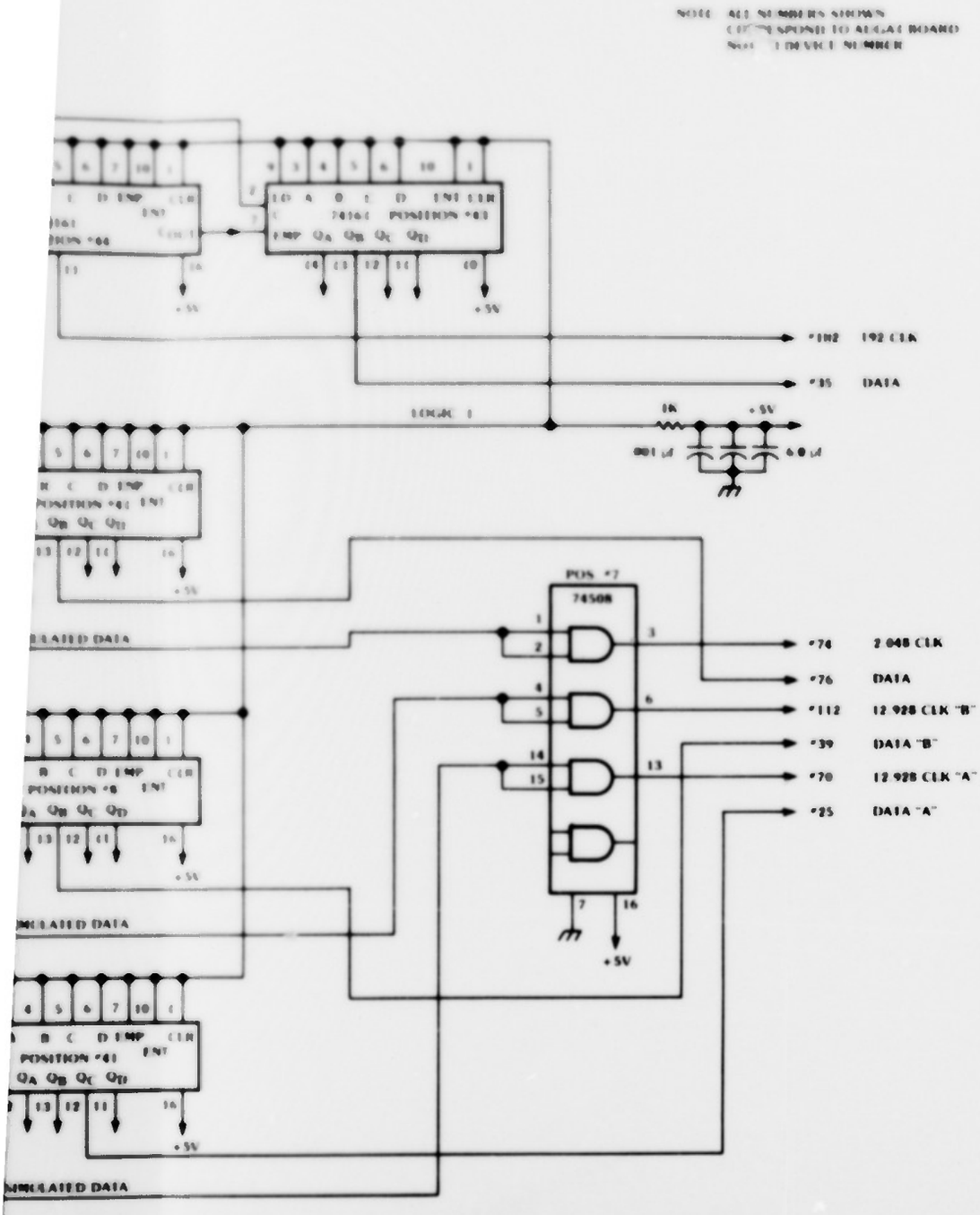
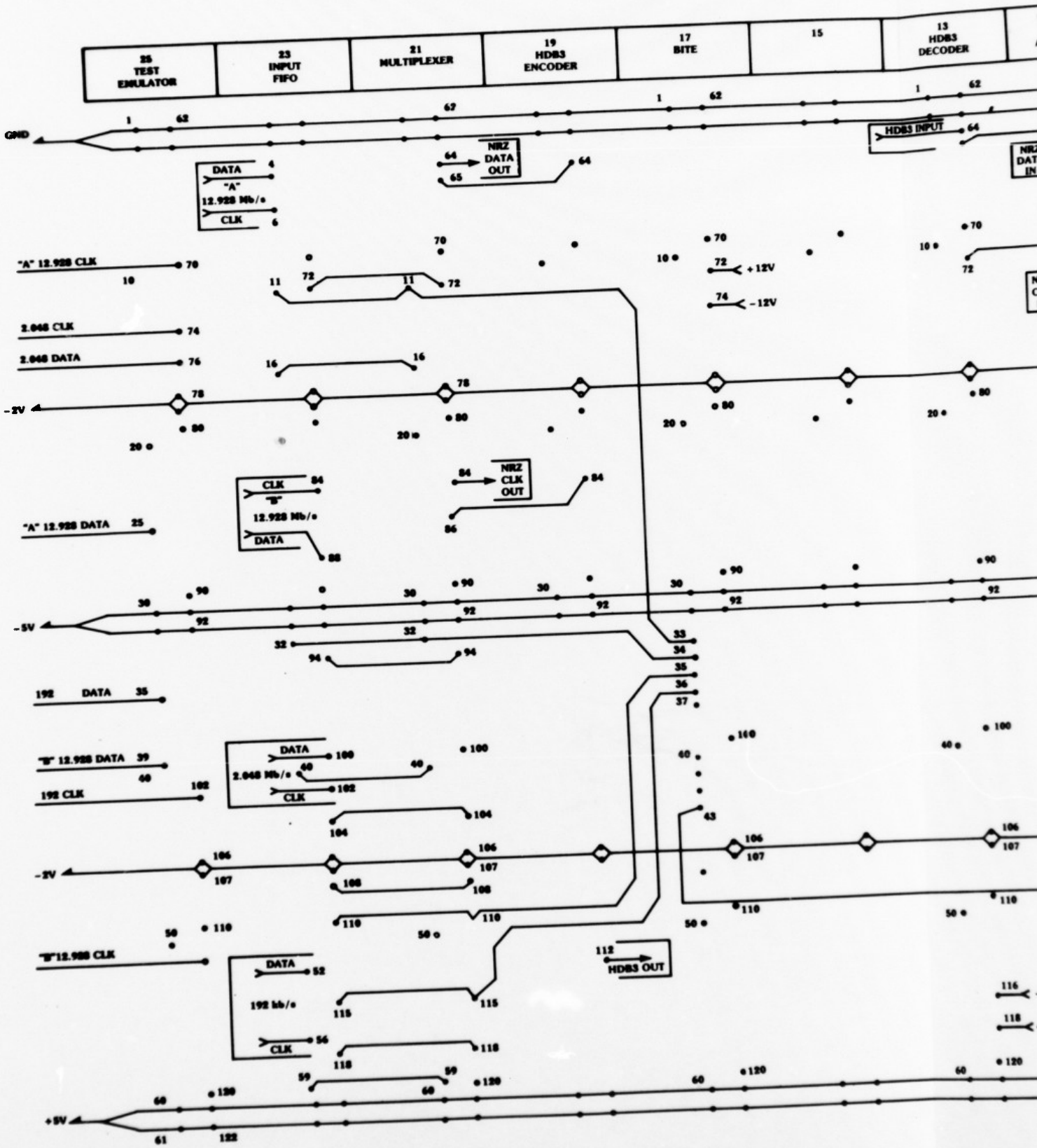


Figure B-9. TEST EMULATOR



B-9. TEST EMULATOR



GND – PINS 1, 2, 17, 18, 45, 46, 62 & 63
+5V – PINS 60, 61, 121 & 122
-5.2V – PINS 30, 31, 91 & 92
-9.0V – PINS 78, 79, 106 & 107

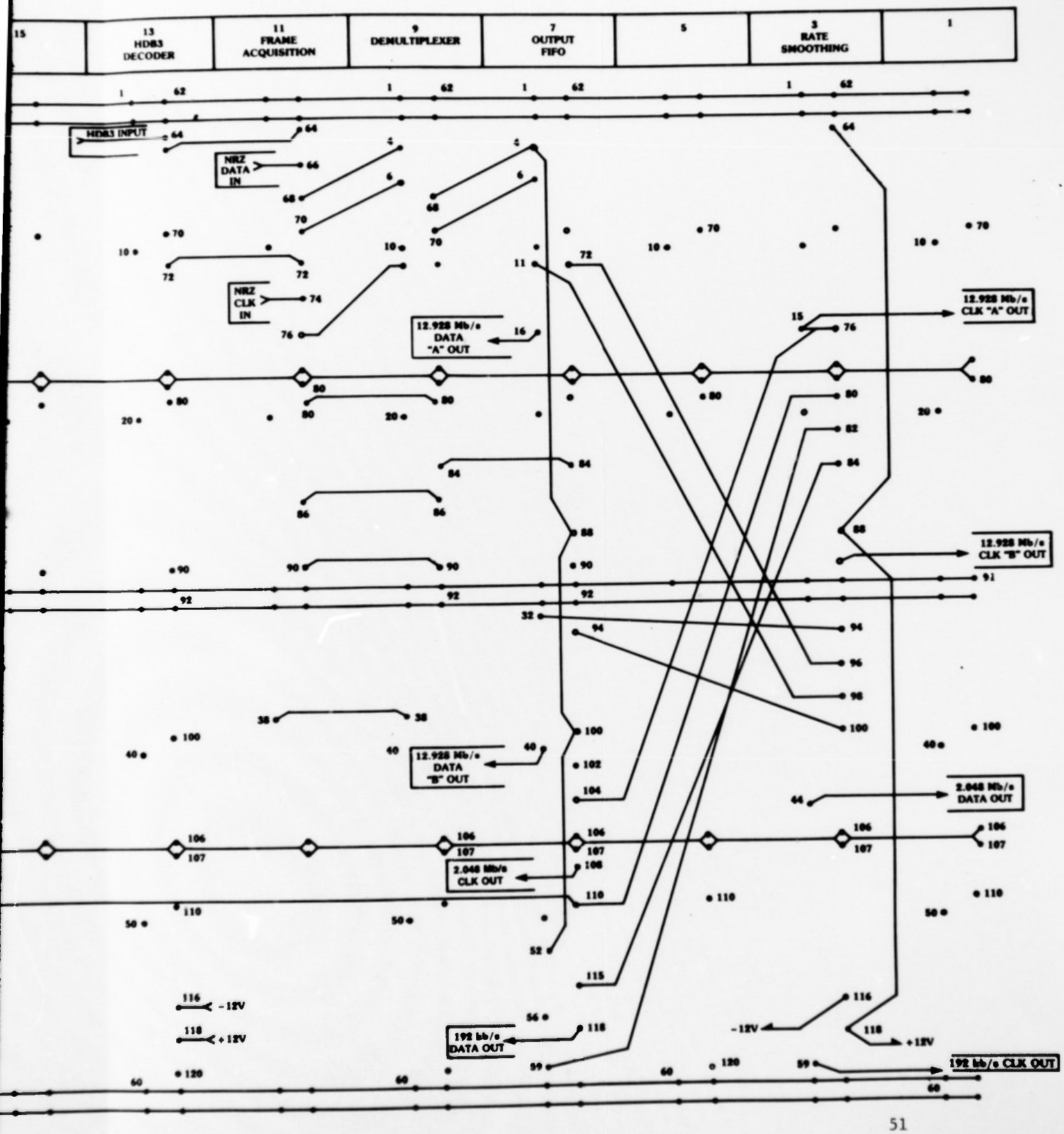


Figure B-10. BACKPANEL WIRING

APPENDIX C

PROGRAMMABLE READ-ONLY MEMORY TRUTH TABLES

Table C-1. MULTIPLEXER, IC (27) (Revised)

Enable Line for True Data, Stuff Control and Stuff Opportunity Times

	Outputs			
Address	D0	D1	D2	D3
0	1	1	0	0
1	1	1	0	0
2	1	1	0	0
3	1	1	0	0
4	1	1	0	1
5	1	1	0	0
6	1	1	0	1
7	1	1	0	1
8	1	1	0	1
9	1	1	0	1
10	1	1	1	1
11	1	1	1	0
12	0	0	0	0
13	0	0	0	1
14	0	0	1	0
15	0	0	0	0
16	0	0	0	1
17	0	0	0	0
18	0	0	0	1
19	0	0	0	0
20	0	0	0	1
21	0	0	0	0
22	0	0	0	1
23	0	0	0	0
24	0	0	0	1
25	0	0	1	0
26	0	0	0	0
27	0	0	0	1
28	0	0	0	0
29	0	0	0	1
30	0	0	0	0
31	0	0	0	1
32	0	0	0	0
33	0	0	0	1
34	0	0	0	0
35	0	0	0	1
36	0	0	0	0
37	0	0	0	1

	Outputs			
Address	D0	D1	D2	D3
38	0	0	0	0
39	0	0	0	1
40	0	0	1	0
41	0	0	0	0
42	0	0	0	1
43	0	0	0	0
44	0	0	0	1
45	0	0	0	0
46	0	0	0	1
47	0	0	0	0
48	0	0	0	1
49	0	0	0	0
50	0	0	0	1
51	0	0	0	0
52	0	0	0	1
53	0	0	1	0
54	0	0	0	0
55	0	0	0	1
56	0	0	0	0
57	0	0	0	1
58	0	0	0	0
59	0	0	0	1
60	0	0	0	0
[illegible]	0	0	0	1
[illegible]	0	0	0	0
63	0	0	0	1
64	0	0	1	0
65	0	0	0	0
66	0	0	0	1
67	0	0	0	0
68	0	0	0	1
69	0	0	0	0
70	0	0	0	1
71	1	1	1	1
72	0	0	0	0
73	0	0	0	1
74	1	1	1	1
75	0	0	0	0

Table C-1. (Continued)

Address	Outputs D0	D1	D2	D3	Address	Outputs D0	D1	D2	D3
76	0	0	0	1	117	0	0	0	0
77	0	0	0	0	118	0	0	0	1
78	0	0	0	1	119	1	1	1	1
79	0	0	1	0	120	0	0	0	0
80	0	0	0	0	121	0	0	0	1
81	0	0	0	1	122	0	0	0	0
82	1	1	1	1	123	0	0	0	1
83	0	0	0	0	124	1	1	1	1
84	0	0	0	1	125	0	0	0	0
85	0	0	0	0	126	0	0	0	1
86	0	0	0	1	127	0	0	1	0
87	1	1	1	1	128	0	0	0	0
88	0	0	0	0	129	0	0	0	1
89	0	0	0	1	130	0	0	0	0
90	1	1	1	1	131	0	0	0	1
91	0	0	0	0	132	1	1	1	1
92	0	0	0	1	133	0	0	0	0
93	0	0	0	0	134	0	0	0	1
94	0	0	0	1	135	1	1	1	1
95	0	0	1	0	136	0	0	0	0
96	0	0	0	0	137	0	0	0	1
97	0	0	0	1	138	0	0	0	0
98	1	1	1	1	139	0	0	0	1
99	0	0	0	0	140	1	0	1	1
100	0	0	0	1	141	0	0	0	0
101	0	0	0	0	142	0	0	0	1
102	0	0	0	1	143	0	0	1	0
103	1	1	1	1	144	0	0	0	0
104	0	0	0	0	145	0	0	0	1
105	0	0	0	1	146	0	0	0	0
106	1	1	1	1	147	0	0	0	1
107	0	0	0	0	148	1	0	1	1
108	0	0	0	1	149	0	0	0	0
109	0	0	0	0	150	0	0	0	1
110	0	0	0	1	151	0	0	0	0
111	0	0	1	0	152	0	0	0	1
112	0	0	0	0	153	1	0	1	1
113	0	0	0	1	154	0	0	0	0
114	0	0	0	0	155	0	0	0	1
115	0	0	0	1	156	1	1	1	1
116	0	0	1	1	157	0	0	0	0

Table C-1. (Continued)

Address	Outputs D0	D1	D2	D3
158	0	0	0	1
159	0	0	0	0
160	0	0	0	1
161	0	0	1	0
162	0	0	0	0
163	0	0	0	1
164	1	1	1	1
165	0	0	0	0
166	0	0	0	1
167	1	0	1	0
168	0	0	0	0
169	0	0	0	1
170	0	0	0	0
171	0	0	0	1
172	1	0	1	0
173	0	0	0	0
174	0	0	0	1
175	1	0	1	0
176	0	0	0	0
177	0	0	0	1
178	0	0	0	0
179	0	0	0	1
180	0	0	1	0
181	0	0	0	0
182	0	0	0	1
183	1	1	1	1
184	0	0	0	0
185	0	0	0	1
186	0	0	0	0
187	0	0	0	1
188	1	1	1	1
189	0	0	0	0
190	0	0	0	1
191	1	0	0	1
192	0	0	0	0
193	0	0	0	1
194	0	0	0	0
195	0	0	0	1
196	0	0	1	0
197	0	0	0	0
198	0	0	0	1
199	1	0	0	1
200	0	0	0	0
201	0	0	0	1
202	0	0	0	0
203	0	0	0	1
204	1	0	0	1
205	0	0	0	0
206	0	0	0	1
207	1	1	1	1
208	0	0	0	0
209	0	0	0	1
210	0	0	0	0
211	0	0	0	1
212	1	1	1	1
213	0	0	0	0
214	0	0	0	1
215	1	0	0	0
216	0	0	0	0
217	0	0	0	1
218	0	0	0	0
219	0	0	0	1
220	0	0	1	0
221	0	0	0	0
222	0	0	0	1
223	1	0	0	0
224	0	0	0	0
225	0	0	0	1
226	0	0	0	0
227	0	0	0	1
228	1	0	0	0
229	0	0	0	0
230	0	0	0	1
231	1	1	1	1
232	0	0	0	0
233	0	0	0	1
234	0	0	0	0
235	0	0	0	1
236	0	0	1	0
237	0	0	0	0
238	0	0	0	1
239	1	1	1	1

Table C-1. (Concluded)

Address	Outputs D0	D1	D2	D3
240	0	0	0	0
241	0	0	0	1
242	0	0	0	0
243	0	0	0	1
244	0	0	1	1
245	0	0	0	0
246	0	0	0	1
247	0	0	1	0

Address	Outputs D0	D1	D2	D3
248	0	0	0	0
249	0	0	0	1
250	0	0	0	0
251	0	0	0	1
252	0	0	0	0
253	0	0	0	1
254	0	0	0	0
255	0	0	0	1

Table C-2. MULTIPLEXER, IC (51) (Revised)

Enable Line for True Data Times

	Outputs			
Address	D0	D1	D2	D3
0	1	1	1	1
1	1	1	1	1
2	1	1	1	1
3	1	1	1	1
4	1	1	1	1
5	1	1	1	1
6	1	1	1	1
7	1	1	1	1
8	1	1	1	1
9	1	1	1	1
10	1	1	1	1
11	1	1	1	1
12	0	0	0	1
13	0	0	1	1
14	0	1	0	1
15	0	0	0	1
16	0	0	1	1
17	0	0	0	1
18	0	0	1	1
19	0	0	0	1
20	0	0	1	1
21	0	0	0	1
22	0	0	1	1
23	0	0	0	1
24	0	0	1	1
25	0	1	0	1
26	0	0	0	1
27	0	0	1	1
28	0	0	0	1
29	0	0	1	1
30	0	0	0	1
31	0	0	1	1
32	0	0	0	1
33	0	0	1	1
34	0	0	0	1
35	0	0	1	1
36	0	0	0	1
37	0	0	1	1
38	0	0	0	1
39	0	0	1	1
40	0	1	0	1
41	0	0	0	1
42	0	0	1	1
43	0	0	0	1
44	0	0	1	1
45	0	0	0	1
46	0	0	1	1
47	0	0	0	1
48	0	0	1	1
49	0	0	0	1
50	0	0	1	1
51	0	0	0	1
52	0	0	1	1
53	0	1	0	1
54	0	0	0	1
55	0	0	1	1
56	0	0	0	1
57	0	0	1	1
58	0	0	0	1
59	0	0	1	1
60	0	0	0	1
61	0	0	1	1
62	0	0	0	1
63	0	0	1	1
64	0	1	0	1
65	0	0	0	1
66	0	0	1	1
67	0	0	0	1
68	0	0	1	1
69	0	0	0	1
70	0	0	1	1
71	1	1	1	1
72	0	0	0	1
73	0	0	1	1
74	1	1	1	1
75	0	0	0	1
76	0	0	1	1
77	0	0	0	1

Table C-2. (Continued)

Address	Outputs D0	D1	D2	D3
78	0	0	1	1
79	0	1	0	1
80	0	0	0	1
81	0	0	1	1
82	1	1	1	1
83	0	0	0	1
84	0	0	1	1
85	0	0	0	1
86	0	0	1	1
87	1	1	1	1
88	0	0	0	1
89	0	0	1	1
90	1	1	1	1
91	0	0	0	1
92	0	0	1	1
93	0	0	0	1
94	0	0	1	1
95	0	1	0	1
96	0	0	0	1
97	0	0	1	1
98	1	1	1	1
99	0	0	0	1
100	0	0	1	1
101	0	0	0	1
102	0	0	1	1
103	1	1	1	1
104	0	0	0	1
105	0	0	1	1
106	1	1	1	1
107	0	0	0	1
108	0	0	1	1
109	0	0	0	1
110	0	0	1	1
111	0	1	0	1
112	0	0	0	1
113	0	0	1	1
114	0	0	0	1
115	0	0	1	1
116	0	1	1	1
117	0	0	0	1
118	0	0	1	1

Address	Outputs D0	D1	D2	D3
119	1	1	1	1
120	0	0	0	1
121	0	0	1	1
122	0	0	0	1
123	0	0	1	1
124	1	1	1	1
125	0	0	0	1
126	0	0	1	1
127	0	1	0	1
128	0	0	0	1
129	0	0	1	1
130	0	0	0	1
131	0	0	1	1
132	1	1	1	1
133	0	0	0	1
134	0	0	1	1
135	1	1	1	1
136	0	0	0	1
137	0	0	1	1
138	0	0	0	1
139	0	0	1	1
140	1	1	1	1
141	0	0	0	1
142	0	0	1	1
143	0	1	0	1
144	0	0	0	1
145	0	0	1	1
146	0	0	0	1
147	0	0	1	1
148	1	1	1	1
149	0	0	0	1
150	0	0	1	1
151	0	0	0	1
152	0	0	1	1
153	1	1	1	1
154	0	0	0	1
155	0	0	1	1
156	1	1	1	1
157	0	0	0	1
158	0	0	1	1
159	0	0	0	1

Table C-2. (Continued)

Address	Outputs D0	D1	D2	D3
160	0	0	1	1
161	0	1	0	1
162	0	0	0	1
163	0	0	1	1
164	1	1	1	1
165	0	0	0	1
166	0	0	1	1
167	1	1	1	1
168	0	0	0	1
169	0	0	1	1
170	0	0	0	1
171	0	0	1	1
172	1	1	1	1
173	0	0	0	1
174	0	0	1	1
175	1	1	1	1
176	0	0	0	1
177	0	0	1	1
178	0	0	0	1
179	0	0	1	1
180	0	1	0	1
181	0	0	0	1
182	0	0	1	1
183	1	1	1	1
184	0	0	0	1
185	0	0	1	1
186	0	0	0	1
187	0	0	1	1
188	1	1	1	1
189	0	0	0	1
190	0	0	1	1
191	1	1	1	1
192	0	0	0	1
193	0	0	1	1
194	0	0	0	1
195	0	0	1	1
196	0	1	0	1
197	0	0	0	1
198	0	0	1	1
199	1	1	1	1
200	0	0	0	1

Address	Outputs D0	D1	D2	D3
201	0	0	1	1
202	0	0	0	1
203	0	0	1	1
204	1	1	1	1
205	0	0	0	1
206	0	0	1	1
207	1	1	1	1
208	0	0	0	1
209	0	0	1	1
210	0	0	0	1
211	0	0	1	1
212	1	1	1	1
213	0	0	0	1
214	0	0	1	1
215	1	1	1	1
216	0	0	0	1
217	0	0	1	1
218	0	0	0	1
219	0	0	1	1
220	0	1	0	1
221	0	0	0	1
222	0	0	1	1
223	1	1	1	1
224	0	0	0	1
225	0	0	1	1
226	0	0	0	1
227	0	0	1	1
228	1	1	1	1
229	0	0	0	1
230	0	0	1	1
231	1	1	1	1
232	0	0	0	1
233	0	0	1	1
234	0	0	0	1
235	0	0	1	1
236	0	1	0	1
237	0	0	0	1
238	0	0	1	1
239	1	1	1	1
240	0	0	0	1
241	0	0	1	1

Table C-2. (Concluded)

Address	Outputs D0	D1	D2	D3
242	0	0	0	1
243	0	0	1	1
244	1	1	1	1
245	0	0	0	1
246	0	0	1	1
247	1	1	1	1
248	0	0	0	1
249	0	0	1	1
250	0	0	0	1
251	0	0	1	1
252	0	0	0	1
253	0	0	1	1
254	1	1	1	1
255	1	1	1	1

Table C-3. MULTIPLEXER, IC (39)

Enable Line for Stuff Opportunity Times

	Outputs			
Address	D0	D1	D2	D3
0	1	1	1	1
1	1	1	1	1
2	1	1	1	1
3	1	1	1	1
4	1	1	1	1
5	1	1	1	1
6	1	1	1	1
7	1	1	1	1
8	1	1	1	1
9	1	1	1	1
10	1	1	1	1
11	1	1	1	1
12	1	1	1	1
13	1	1	1	1
14	1	1	1	1
15	1	1	1	1
16	1	1	1	1
17	1	1	1	1
18	1	1	1	1
19	1	1	1	1
20	1	1	1	1
21	1	1	1	1
22	1	1	1	1
23	1	1	1	1
24	1	1	1	1
25	1	1	1	1
26	1	1	1	1
27	1	1	1	1
28	1	1	1	1
29	1	1	1	1
30	1	1	1	1
31	1	1	1	1
32	1	1	1	1
33	1	1	1	1
34	1	1	1	1
35	1	1	1	1
36	1	1	1	1
37	1	1	1	1
38	1	1	1	1

	Outputs			
Address	D0	D1	D2	D3
39	1	1	1	1
40	1	1	1	1
41	1	1	1	1
42	1	1	1	1
43	1	1	1	1
44	1	1	1	1
45	1	1	1	1
46	1	1	1	1
47	1	1	1	1
48	1	1	1	1
49	1	1	1	1
50	1	1	1	1
51	1	1	1	1
52	1	1	1	1
53	1	1	1	1
54	1	1	1	1
55	1	1	1	1
56	1	1	1	1
57	1	1	1	1
58	1	1	1	1
59	1	1	1	1
60	1	1	1	1
61	1	1	1	1
62	1	1	1	1
63	1	1	1	1
64	1	1	1	1
65	1	1	1	1
66	1	1	1	1
67	1	1	1	1
68	1	1	1	1
69	1	1	1	1
70	1	1	1	1
71	1	1	1	1
72	1	1	1	1
73	1	1	1	1
74	1	1	1	1
75	1	1	1	1
76	1	1	1	1
77	1	1	1	1

Table C-3. (Continued)

Address	Outputs D0	D1	D2	D3
78	1	1	1	1
79	1	1	1	1
80	1	1	1	1
81	1	1	1	1
82	1	1	1	1
83	1	1	1	1
84	1	1	1	1
85	1	1	1	1
86	1	1	1	1
87	1	1	1	1
88	1	1	1	1
89	1	1	1	1
90	1	1	1	1
91	1	1	1	1
92	1	1	1	1
93	1	1	1	1
94	1	1	1	1
95	1	1	1	1
96	1	1	1	1
97	1	1	1	1
98	1	1	1	1
99	1	1	1	1
100	1	1	1	1
101	1	1	1	1
102	1	1	1	1
103	1	1	1	1
104	1	1	1	1
105	1	1	1	1
106	1	1	1	1
107	1	1	1	1
108	1	1	1	1
109	1	1	1	1
110	1	1	1	1
111	1	1	1	1
112	1	1	1	1
113	1	1	1	1
114	1	1	1	1
115	1	1	1	1
116	1	1	1	1
117	1	1	1	1
118	1	1	1	1

Address	Outputs D0	D1	D2	D3
119	1	1	1	1
120	1	1	1	1
121	1	1	1	1
122	1	1	1	1
123	1	1	1	1
124	1	1	1	1
125	1	1	1	1
126	1	1	1	1
127	1	1	1	1
128	1	1	1	1
129	1	1	1	1
130	1	1	1	1
131	1	1	1	1
132	1	1	1	1
133	1	1	1	1
134	1	1	1	1
135	1	1	1	1
136	1	1	1	1
137	1	1	1	1
138	1	1	1	1
139	1	1	1	1
140	1	1	1	1
141	1	1	1	1
142	1	1	1	1
143	1	1	1	1
144	1	1	1	1
145	1	1	1	1
146	1	1	1	1
147	1	1	1	1
148	1	1	1	1
149	1	1	1	1
150	1	1	1	1
151	1	1	1	1
152	1	1	1	1
153	1	1	1	1
154	1	1	1	1
155	1	1	1	1
156	1	1	1	1
157	1	1	1	1
158	1	1	1	1
159	1	1	1	1

Table C-3. (Continued)

Address	Outputs D0	D1	D2	D3
160	1	1	1	1
161	1	1	1	1
162	1	1	1	1
163	1	1	1	1
164	1	1	1	1
165	1	1	1	1
166	1	1	1	1
167	1	1	1	1
168	1	1	1	1
169	1	1	1	1
170	1	1	1	1
171	1	1	1	1
172	1	1	1	1
173	1	1	1	1
174	1	1	1	1
175	1	1	1	1
176	1	1	1	1
177	1	1	1	1
178	1	1	1	1
179	1	1	1	1
180	1	1	1	1
181	1	1	1	1
182	1	1	1	1
183	1	1	1	1
184	1	1	1	1
185	1	1	1	1
186	1	1	1	1
187	1	1	1	1
188	1	1	1	1
189	1	1	1	1
190	1	1	1	1
191	1	1	1	1
192	1	1	1	1
193	1	1	1	1
194	1	1	1	1
195	1	1	1	1
196	1	1	1	1
197	1	1	1	1
198	1	1	1	1
199	1	1	1	1
200	1	1	1	1

Address	Outputs D0	D1	D2	D3
201	1	1	1	1
202	1	1	1	1
203	1	1	1	1
204	1	1	1	1
205	1	1	1	1
206	1	1	1	1
207	1	1	1	1
208	1	1	1	1
209	1	1	1	1
210	1	1	1	1
211	1	1	1	1
212	1	1	1	1
213	1	1	1	1
214	1	1	1	1
215	1	1	1	1
216	1	1	1	1
217	1	1	1	1
218	1	1	1	1
219	1	1	1	1
220	1	1	1	1
221	1	1	1	1
222	1	1	1	1
223	1	1	1	1
224	1	1	1	1
225	1	1	1	1
226	1	1	1	1
227	1	1	1	1
228	1	1	1	1
229	1	1	1	1
230	1	1	1	1
231	1	1	1	1
232	1	1	1	1
233	1	1	1	1
234	1	1	1	1
235	1	1	1	1
236	1	1	1	1
237	1	1	1	1
238	1	1	1	1
239	1	1	1	1
240	1	1	1	1
241	1	1	1	1

Table C-3. (Continued)

Address	Outputs D0	D1	D2	D3
242	1	1	1	1
243	1	1	1	1
244	1	1	0	1
245	1	1	1	1
246	1	1	1	1
247	1	1	1	0
248	1	1	1	1
249	1	1	1	1
250	1	1	1	1
251	1	1	1	1
252	1	1	1	1
253	1	1	1	1
254	1	0	1	1
255	0	1	1	1

Table C-4. DEMULTIPLEXER, IC (27)

Enable Line for True Data Except
Stuff Opportunity Times

	Outputs					Outputs				
Address	D0	D1	D2	D3		Address	D0	D1	D2	D3
0	0	0	0	0		38	1	0	0	0
1	0	0	0	0		39	0	1	0	0
2	0	0	0	0		40	0	0	1	0
3	0	0	0	0		41	1	0	0	0
4	0	0	0	0		42	0	1	0	0
5	0	0	0	0		43	1	0	0	0
6	0	0	0	0		44	0	1	0	0
7	0	0	0	0		45	1	0	0	0
8	0	0	0	0		46	0	1	0	0
9	0	0	0	0		47	1	0	0	0
10	0	0	0	0		48	0	1	0	0
11	0	0	0	0		49	1	0	0	0
12	1	0	0	0		50	0	1	0	0
13	0	1	0	0		51	1	0	0	0
14	0	0	1	0		52	0	1	0	0
15	1	0	0	0		53	0	0	1	0
16	0	1	0	0		54	1	0	0	0
17	1	0	0	0		55	0	1	0	0
18	0	1	0	0		56	1	0	0	0
19	1	0	0	0		57	0	1	0	0
20	0	1	0	0		58	1	0	0	0
21	1	0	0	0		59	0	1	0	0
22	0	1	0	0		60	1	0	0	0
23	1	0	0	0		61	0	1	0	0
24	0	1	0	0		62	1	0	0	0
25	0	0	1	0		63	0	1	0	0
26	1	0	0	0		64	0	0	1	0
27	0	1	0	0		65	1	0	0	0
28	1	0	0	0		66	0	1	0	0
29	0	1	0	0		67	1	0	0	0
30	1	0	0	0		68	0	1	0	0
31	0	1	0	0		69	1	0	0	0
32	1	0	0	0		70	0	1	0	0
33	0	1	0	0		71	0	0	0	0
34	1	0	0	0		72	1	0	0	0
35	0	1	0	0		73	0	1	0	0
36	1	0	0	0		74	0	0	0	0
37	0	1	0	0		75	1	0	0	0

Table C-4. (Continued)

Address	Outputs D0	D1	D2	D3
76	0	1	0	0
77	1	0	0	0
78	0	1	0	0
79	0	0	1	0
80	1	0	0	0
81	0	1	0	0
82	0	0	0	0
83	1	0	0	0
84	0	1	0	0
85	1	0	0	0
86	0	1	0	0
87	0	0	0	0
88	1	0	0	0
89	0	1	0	0
90	0	0	0	0
91	1	0	0	0
92	0	1	0	0
93	1	0	0	0
94	0	1	0	0
95	0	0	1	0
96	1	0	0	0
97	0	1	0	0
98	0	0	0	0
99	1	0	0	0
100	0	1	0	0
101	1	0	0	0
102	0	1	0	0
103	0	0	0	0
104	1	0	0	0
105	0	1	0	0
106	0	0	0	0
107	1	0	0	0
108	0	1	0	0
109	1	0	0	0
110	0	1	0	0
111	0	0	1	0
112	1	0	0	0
113	0	1	0	0
114	1	0	0	0
115	0	1	0	0
116	0	0	0	1

Address	Outputs D0	D1	D2	D3
117	1	0	0	0
118	0	1	0	0
119	0	0	0	0
120	1	0	0	0
121	0	1	0	0
122	1	0	0	0
123	0	1	0	0
124	0	0	0	0
125	1	0	0	0
126	0	1	0	0
127	0	0	1	0
128	1	0	0	0
129	0	1	0	0
130	1	0	0	0
131	0	1	0	0
132	0	0	0	0
133	1	0	0	0
134	0	1	0	0
135	0	0	0	0
136	1	0	0	0
137	0	1	0	0
138	1	0	0	0
139	0	1	0	0
140	0	0	0	0
141	1	0	0	0
142	0	1	0	0
143	0	0	1	0
144	1	0	0	0
145	0	1	0	0
146	1	0	0	0
147	0	1	0	0
148	0	0	0	0
149	1	0	0	0
150	0	1	0	0
151	1	0	0	0
152	0	1	0	0
153	0	0	0	0
154	1	0	0	0
155	0	1	0	0
156	0	0	0	0
157	1	0	0	0

Table C-4. (Continued)

Address	Outputs D0	D1	D2	D3
158	0	1	0	0
159	1	0	0	0
160	0	1	0	0
161	0	0	1	0
162	1	0	0	0
163	0	1	0	0
164	0	0	0	0
165	1	0	0	0
166	0	1	0	0
167	0	0	0	0
168	1	0	0	0
169	0	1	0	0
170	1	0	0	0
171	0	1	0	0
172	0	0	0	0
173	1	0	0	0
174	0	1	0	0
175	0	0	0	0
176	1	0	0	0
177	0	1	0	0
178	1	0	0	0
179	0	1	0	0
180	0	0	1	0
181	1	0	0	0
182	0	1	0	0
183	0	0	0	0
184	1	0	0	0
185	0	1	0	0
186	1	0	0	0
187	0	1	0	0
188	0	0	0	0
189	1	0	0	0
190	0	1	0	0
191	0	0	0	0
192	1	0	0	0
193	0	1	0	0
194	1	0	0	0
195	0	1	0	0
196	0	0	1	0
197	1	0	0	0
198	0	1	0	0
199	0	0	0	0
200	1	0	0	0
201	0	1	0	0
202	1	0	0	0
203	0	1	0	0
204	0	0	0	0
205	1	0	0	0
206	0	1	0	0
207	0	0	0	0
208	1	0	0	0
209	0	1	0	0
210	1	0	0	0
211	0	1	0	0
212	0	0	0	0
213	1	0	0	0
214	0	1	0	0
215	0	0	0	0
216	1	0	0	0
217	0	1	0	0
218	1	0	0	0
219	0	1	0	0
220	0	0	1	0
221	1	0	0	0
222	0	1	0	0
223	0	0	0	0
224	1	0	0	0
225	0	1	0	0
226	1	0	0	0
227	0	1	0	0
228	0	0	0	0
229	1	0	0	0
230	0	1	0	0
231	0	0	0	0
232	1	0	0	0
233	0	1	0	0
234	1	0	0	0
235	0	1	0	0
236	0	0	1	0
237	1	0	0	0
238	0	1	0	0
239	0	0	0	0

Table C-4. (Concluded)

Address	Outputs D0	D1	D2	D3
240	1	0	0	0
241	0	1	0	0
242	1	0	0	0
243	0	1	0	0
244	0	0	0	0
245	1	0	0	0
246	0	1	0	0
247	0	0	0	0

Address	Outputs D0	D1	D2	D3
248	1	0	0	0
249	0	1	0	0
250	1	0	0	0
251	0	1	0	0
252	1	0	0	0
253	0	1	0	0
254	0	0	0	0
255	0	0	0	0

Table C-5. DEMULTIPLEXER, IC (50) (Revision 2)

"10" Detect

	Output			
Address	D0	D1	D2	D3
0	0	0	0	0
1	0	0	0	0
2	0	0	0	0
3	0	0	0	0
4	0	0	0	0
5	0	0	0	0
6	0	0	0	0
7	0	0	0	1
8	0	0	1	0
9	0	1	0	0
10	1	0	0	0
11	0	0	0	0
12	0	0	0	0
13	0	0	0	0
14	0	0	0	0
15	0	0	0	0
16	0	0	0	0
17	0	0	0	0
18	0	0	0	0
19	0	0	0	0
20	0	0	0	0
21	0	0	0	0
22	0	0	0	0
23	0	0	0	0
24	0	0	0	0
25	0	0	0	0
26	0	0	0	0
27	0	0	0	0
28	0	0	0	0
29	0	0	0	0
30	0	0	0	0
31	0	0	0	0
32	0	0	0	0
33	0	0	0	0
34	0	0	0	0
35	0	0	0	0
36	0	0	0	0
37	0	0	0	0
38	0	0	0	0

	Output			
Address	D0	D1	D2	D3
39	0	0	0	0
40	0	0	0	0
41	0	0	0	0
42	0	0	0	0
43	0	0	0	0
44	0	0	0	0
45	0	0	0	0
46	0	0	0	0
47	0	0	0	0
48	0	0	0	0
49	0	0	0	0
50	0	0	0	0
51	0	0	0	0
52	0	0	0	0
53	0	0	0	0
54	0	0	0	0
55	0	0	0	0
56	0	0	0	0
57	0	0	0	0
58	0	0	0	0
59	0	0	0	0
60	0	0	0	0
61	0	0	0	0
62	0	0	0	0
63	0	0	0	0
64	0	0	0	0
65	0	0	0	0
66	0	0	0	0
67	0	0	0	0
68	0	0	0	0
69	0	0	0	0
70	0	0	0	0
71	0	0	0	0
72	0	0	0	0
73	0	0	0	0
74	0	0	0	0
75	0	0	0	0
76	0	0	0	0
77	0	0	0	0

Table C-5. (Continued)

Address	Output D0	D1	D2	D3
78	0	0	0	0
79	0	0	0	0
80	0	0	0	0
81	0	0	0	0
82	0	0	0	0
83	0	0	0	0
84	0	0	0	0
85	0	0	0	0
86	0	0	0	0
87	0	0	0	0
88	0	0	0	0
89	0	0	0	0
90	0	0	0	0
91	0	0	0	0
92	0	0	0	0
93	0	0	0	0
94	0	0	0	0
95	0	0	0	0
96	0	0	0	0
97	0	0	0	0
98	0	0	0	0
99	0	0	0	0
100	0	0	0	0
101	0	0	0	0
102	0	0	0	0
103	0	0	0	0
104	0	0	0	0
105	0	0	0	0
106	0	0	0	0
107	0	0	0	0
108	0	0	0	0
109	0	0	0	0
110	0	0	0	0
111	0	0	0	0
112	0	0	0	0
113	0	0	0	0
114	0	0	0	0
115	0	0	0	0
116	0	0	0	0
117	0	0	0	0
118	0	0	0	0

Address	Output D0	D1	D2	D3
119	0	0	0	0
120	0	0	0	0
121	0	0	0	0
122	0	0	0	0
123	0	0	0	0
124	0	0	0	0
125	0	0	0	0
126	0	0	0	0
127	0	0	0	0
128	0	0	0	0
129	0	0	0	0
130	0	0	0	0
131	0	0	0	0
132	0	0	0	0
133	0	0	0	0
134	0	0	0	0
135	0	0	0	0
136	0	0	0	0
137	0	0	0	0
138	0	0	0	0
139	0	0	0	0
140	0	0	0	0
141	0	0	0	0
142	0	0	0	0
143	0	0	0	0
144	0	0	0	0
145	0	0	0	0
146	0	0	0	0
147	0	0	0	0
148	0	0	0	0
149	0	0	0	0
150	0	0	0	0
151	0	0	0	0
152	0	0	0	0
153	0	0	0	0
154	0	0	0	0
155	0	0	0	0
156	0	0	0	0
157	0	0	0	0
158	0	0	0	0
159	0	0	0	0

Table C-5. (Continued)

Address	Output D0	D1	D2	D3
160	0	0	0	0
161	0	0	0	0
162	0	0	0	0
163	0	0	0	0
164	0	0	0	0
165	0	0	0	0
166	0	0	0	0
167	0	0	0	0
168	0	0	0	0
169	0	0	0	0
170	0	0	0	0
171	0	0	0	0
172	0	0	0	0
173	0	0	0	0
174	0	0	0	0
175	0	0	0	0
176	0	0	0	0
177	0	0	0	0
178	0	0	0	0
179	0	0	0	0
180	0	0	0	0
181	0	0	0	0
182	0	0	0	0
183	0	0	0	0
184	0	0	0	0
185	0	0	0	0
186	0	0	0	0
187	0	0	0	0
188	0	0	0	0
189	0	0	0	0
190	0	0	0	0
191	0	0	0	0
192	0	0	0	0
193	0	0	0	0
194	0	0	0	0
195	0	0	0	0
196	0	0	0	0
197	0	0	0	0
198	0	0	0	0
199	0	0	0	0
200	0	0	0	0

Address	Output D0	D1	D2	D3
201	0	0	0	0
202	0	0	0	0
203	0	0	0	0
204	0	0	0	0
205	0	0	0	0
206	0	0	0	0
207	0	0	0	0
208	0	0	0	0
209	0	0	0	0
210	0	0	0	0
211	0	0	0	0
212	0	0	0	0
213	0	0	0	0
214	0	0	0	0
215	0	0	0	0
216	0	0	0	0
217	0	0	0	0
218	0	0	0	0
219	0	0	0	0
220	0	0	0	0
221	0	0	0	0
222	0	0	0	0
223	0	0	0	0
224	0	0	0	0
225	0	0	0	0
226	0	0	0	0
227	0	0	0	0
228	0	0	0	0
229	0	0	0	0
230	0	0	0	0
231	0	0	0	0
232	0	0	0	0
233	0	0	0	0
234	0	0	0	0
235	0	0	0	0
236	0	0	0	0
237	0	0	0	0
238	0	0	0	0
239	0	0	0	0
240	0	0	0	0
241	0	0	0	0

Table C-5. (Concluded)

Address	Output D0	D1	D2	D3
242	0	0	0	0
243	0	0	0	0
244	0	0	0	0
245	0	0	0	0
246	0	0	0	0
247	0	0	0	0
248	0	0	0	0
249	0	0	0	0
250	0	0	0	0
251	0	0	0	0
252	0	0	0	0
253	0	0	0	0
254	0	0	0	0
255	0	0	0	0

Table C-6. DEMULTIPLEXER, IC (51)

Enable Line For Stuff Opportunity Times

	Outputs			
Address	D0	D1	D2	D3
0	0	0	0	0
1	0	0	0	0
2	0	0	0	0
3	0	0	0	0
4	0	0	0	0
5	0	0	0	0
6	0	0	0	0
7	0	0	0	0
8	0	0	0	0
9	0	0	0	0
10	0	0	0	0
11	0	0	0	0
12	0	0	0	0
13	0	0	0	0
14	0	0	0	0
15	0	0	0	0
16	0	0	0	0
17	0	0	0	0
18	0	0	0	0
19	0	0	0	0
20	0	0	0	0
21	0	0	0	0
22	0	0	0	0
23	0	0	0	0
24	0	0	0	0
25	0	0	0	0
26	0	0	0	0
27	0	0	0	0
28	0	0	0	0
29	0	0	0	0
30	0	0	0	0
31	0	0	0	0
32	0	0	0	0
33	0	0	0	0
34	0	0	0	0
35	0	0	0	0
36	0	0	0	0
37	0	0	0	0
38	0	0	0	0

	Outputs			
Address	D0	D1	D2	D3
39	0	0	0	0
40	0	0	0	0
41	0	0	0	0
42	0	0	0	0
43	0	0	0	0
44	0	0	0	0
45	0	0	0	0
46	0	0	0	0
47	0	0	0	0
48	0	0	0	0
49	0	0	0	0
50	0	0	0	0
51	0	0	0	0
52	0	0	0	0
53	0	0	0	0
54	0	0	0	0
55	0	0	0	0
56	0	0	0	0
57	0	0	0	0
58	0	0	0	0
59	0	0	0	0
60	0	0	0	0
61	0	0	0	0
62	0	0	0	0
63	0	0	0	0
64	0	0	0	0
65	0	0	0	0
66	0	0	0	0
67	0	0	0	0
68	0	0	0	0
69	0	0	0	0
70	0	0	0	0
71	0	0	0	0
72	0	0	0	0
73	0	0	0	0
74	0	0	0	0
75	0	0	0	0
76	0	0	0	0
77	0	0	0	0

Table C-6. (Continued)

Address	Outputs D0	D1	D2	D3
78	0	0	0	0
79	0	0	0	0
80	0	0	0	0
81	0	0	0	0
82	0	0	0	0
83	0	0	0	0
84	0	0	0	0
85	0	0	0	0
86	0	0	0	0
87	0	0	0	0
88	0	0	0	0
89	0	0	0	0
90	0	0	0	0
91	0	0	0	0
92	0	0	0	0
93	0	0	0	0
94	0	0	0	0
95	0	0	0	0
96	0	0	0	0
97	0	0	0	0
98	0	0	0	0
99	0	0	0	0
100	0	0	0	0
101	0	0	0	0
102	0	0	0	0
103	0	0	0	0
104	0	0	0	0
105	0	0	0	0
106	0	0	0	0
107	0	0	0	0
108	0	0	0	0
109	0	0	0	0
110	0	0	0	0
111	0	0	0	0
112	0	0	0	0
113	0	0	0	0
114	0	0	0	0
115	0	0	0	0
116	0	0	0	0
117	0	0	0	0
118	0	0	0	0
119	0	0	0	0
120	0	0	0	0
121	0	0	0	0
122	0	0	0	0
123	0	0	0	0
124	0	0	0	0
125	0	0	0	0
126	0	0	0	0
127	0	0	0	0
128	0	0	0	0
129	0	0	0	0
130	0	0	0	0
131	0	0	0	0
132	0	0	0	0
133	0	0	0	0
134	0	0	0	0
135	0	0	0	0
136	0	0	0	0
137	0	0	0	0
138	0	0	0	0
139	0	0	0	0
140	0	0	0	0
141	0	0	0	0
142	0	0	0	0
143	0	0	0	0
144	0	0	0	0
145	0	0	0	0
146	0	0	0	0
147	0	0	0	0
148	0	0	0	0
149	0	0	0	0
150	0	0	0	0
151	0	0	0	0
152	0	0	0	0
153	0	0	0	0
154	0	0	0	0
155	0	0	0	0
156	0	0	0	0
157	0	0	0	0
158	0	0	0	0
159	0	0	0	0

Table C-6. (Continued)

Address	Outputs D0	D1	D2	D3
160	0	0	0	0
161	0	0	0	0
162	0	0	0	0
163	0	0	0	0
164	0	0	0	0
165	0	0	0	0
166	0	0	0	0
167	0	0	0	0
168	0	0	0	0
169	0	0	0	0
170	0	0	0	0
171	0	0	0	0
172	0	0	0	0
173	0	0	0	0
174	0	0	0	0
175	0	0	0	0
176	0	0	0	0
177	0	0	0	0
178	0	0	0	0
179	0	0	0	0
180	0	0	0	0
181	0	0	0	0
182	0	0	0	0
183	0	0	0	0
184	0	0	0	0
185	0	0	0	0
186	0	0	0	0
187	0	0	0	0
188	0	0	0	0
189	0	0	0	0
190	0	0	0	0
191	0	0	0	0
192	0	0	0	0
193	0	0	0	0
194	0	0	0	0
195	0	0	0	0
196	0	0	0	0
197	0	0	0	0
198	0	0	0	0
199	0	0	0	0
200	0	0	0	0

Address	Outputs D0	D1	D2	D3
201	0	0	0	0
202	0	0	0	0
203	0	0	0	0
204	0	0	0	0
205	0	0	0	0
206	0	0	0	0
207	0	0	0	0
208	0	0	0	0
209	0	0	0	0
210	0	0	0	0
211	0	0	0	0
212	0	0	0	0
213	0	0	0	0
214	0	0	0	0
215	0	0	0	0
216	0	0	0	0
217	0	0	0	0
218	0	0	0	0
219	0	0	0	0
220	0	0	0	0
221	0	0	0	0
222	0	0	0	0
223	0	0	0	0
224	0	0	0	0
225	0	0	0	0
226	0	0	0	0
227	0	0	0	0
228	0	0	0	0
229	0	0	0	0
230	0	0	0	0
231	0	0	0	0
232	0	0	0	0
233	0	0	0	0
234	0	0	0	0
235	0	0	0	0
236	0	0	0	0
237	0	0	0	0
238	0	0	0	0
239	0	0	0	0
240	0	0	0	0
241	0	0	0	0

Table C-6. (Concluded)

	Outputs			
Address	D0	D1	D2	D3
242	0	0	0	0
243	0	0	0	0
244	0	0	0	1
245	0	0	0	0
246	0	0	0	0
247	0	0	1	0
248	0	0	0	0

	Outputs			
Address	D0	D1	D2	D3
249	0	0	0	0
250	0	0	0	0
251	0	0	0	0
252	0	0	0	0
253	0	0	0	0
254	1	0	0	0
255	0	1	0	0

Table C-7. DEMULTIPLEXER, IC (53)

Enable Line For Stuff Control Times

	Outputs			
Address	D0	D1	D2	D3
0	0	0	0	0
1	0	0	0	0
2	0	0	0	0
3	0	0	0	0
4	0	0	0	0
5	0	0	0	0
6	0	0	0	0
7	0	0	0	0
8	0	0	0	0
9	0	0	0	0
10	0	0	0	0
11	0	0	0	0
12	0	0	0	0
13	0	0	0	0
14	0	0	0	0
15	0	0	0	0
16	0	0	0	0
17	0	0	0	0
18	0	0	0	0
19	0	0	0	0
20	0	0	0	0
21	0	0	0	0
22	0	0	0	0
23	0	0	0	0
24	0	0	0	0
25	0	0	0	0
26	0	0	0	0
28	0	0	0	0
29	0	0	0	0
30	0	0	0	0
31	0	0	0	0
32	0	0	0	0
33	0	0	0	0
34	0	0	0	0
35	0	0	0	0
36	0	0	0	0
37	0	0	0	0
38	0	0	0	0
39	0	0	0	0

	Outputs			
Address	D0	D1	D2	D3
40	0	0	0	0
41	0	0	0	0
42	0	0	0	0
43	0	0	0	0
44	0	0	0	0
45	0	0	0	0
46	0	0	0	0
47	0	0	0	0
48	0	0	0	0
49	0	0	0	0
50	0	0	0	0
51	0	0	0	0
52	0	0	0	0
53	0	0	0	0
54	0	0	0	0
55	0	0	0	0
56	0	0	0	0
57	0	0	0	0
58	0	0	0	0
59	0	0	0	0
60	0	0	0	0
61	0	0	0	0
62	0	0	0	0
63	0	0	0	0
64	0	0	0	0
65	0	0	0	0
66	0	0	0	0
67	0	0	0	0
68	0	0	0	0
69	0	0	0	0
70	0	0	0	0
71	0	0	0	0
72	0	0	0	0
73	0	0	0	0
74	0	0	0	0
75	0	0	0	0
76	0	0	0	0
77	0	0	0	0
78	0	0	0	0

Table C-7. (Continued)

Address	Outputs D0	D1	D2	D3
79	0	0	0	0
80	0	0	0	0
81	0	0	0	0
82	0	0	0	0
83	0	0	0	0
84	0	0	0	0
85	0	0	0	0
86	0	0	0	0
87	0	0	0	0
88	0	0	0	0
89	0	0	0	0
90	0	0	0	0
91	0	0	0	0
92	0	0	0	0
93	0	0	0	0
94	0	0	0	0
95	0	0	0	0
96	0	0	0	0
97	0	0	0	0
98	0	0	0	0
99	0	0	0	0
100	0	0	0	0
101	0	0	0	0
102	0	0	0	0
103	0	0	0	0
104	0	0	0	0
105	0	0	0	0
106	0	0	0	0
107	0	0	0	0
108	0	0	0	0
109	0	0	0	0
110	0	0	0	0
111	0	0	0	0
112	0	0	0	0
113	0	0	0	0
114	0	0	0	0
115	0	0	0	0
116	0	0	0	0
117	0	0	0	0
118	0	0	0	0
119	0	0	0	0

Address	Outputs D0	D1	D2	D3
120	0	0	0	0
121	0	0	0	0
122	0	0	0	0
123	0	0	0	0
124	0	0	0	0
125	0	0	0	0
126	0	0	0	0
127	0	0	0	0
128	0	0	0	0
129	0	0	0	0
130	0	0	0	0
131	0	0	0	0
132	0	0	0	0
133	0	0	0	0
134	0	0	0	0
135	0	0	0	0
136	0	0	0	0
137	0	0	0	0
138	0	0	0	0
139	0	0	0	0
140	0	0	0	1
141	0	0	0	0
142	0	0	0	0
143	0	0	0	0
144	0	0	0	0
145	0	0	0	0
146	0	0	0	0
147	0	0	0	0
148	0	0	0	1
149	0	0	0	0
150	0	0	0	0
151	0	0	0	0
152	0	0	0	0
153	0	0	0	1
154	0	0	0	0
155	0	0	0	0
156	0	0	0	0
157	0	0	0	0
158	0	0	0	0
159	0	0	0	0
160	0	0	0	0

Table C-7. (Continued)

Address	Outputs D0	D1	D2	D3
161	0	0	0	0
162	0	0	0	0
163	0	0	0	0
164	0	0	0	0
165	0	0	0	0
166	0	0	0	0
167	0	0	1	0
168	0	0	0	0
169	0	0	0	0
170	0	0	0	0
171	0	0	0	0
172	0	0	1	0
173	0	0	0	0
174	0	0	0	0
175	0	0	1	0
176	0	0	0	0
177	0	0	0	0
178	0	0	0	0
179	0	0	0	0
180	0	0	0	0
181	0	0	0	0
182	0	0	0	0
183	0	0	0	0
184	0	0	0	0
185	0	0	0	0
186	0	0	0	0
187	0	0	0	0
188	0	0	0	0
189	0	0	0	0
190	0	0	0	0
191	0	1	0	0
192	0	0	0	0
193	0	0	0	0
194	0	0	0	0
195	0	0	0	0
196	0	0	0	0
197	0	0	0	0
198	0	0	0	0
199	0	1	0	0
200	0	0	0	0
201	0	0	0	0

Address	Outputs D0	D1	D2	D3
202	0	0	0	0
203	0	0	0	0
204	0	1	0	0
205	0	0	0	0
206	0	0	0	0
207	0	0	0	0
208	0	0	0	0
209	0	0	0	0
210	0	0	0	0
211	0	0	0	0
212	0	0	0	0
213	0	0	0	0
214	0	0	0	0
215	1	0	0	0
216	0	0	0	0
217	0	0	0	0
218	0	0	0	0
219	0	0	0	0
220	0	0	0	0
221	0	0	0	0
222	0	0	0	0
223	1	0	0	0
224	0	0	0	0
225	0	0	0	0
226	0	0	0	0
227	0	0	0	0
228	1	0	0	0
229	0	0	0	0
230	0	0	0	0
231	0	0	0	0
232	0	0	0	0
233	0	0	0	0
234	0	0	0	0
235	0	0	0	0
236	0	0	0	0
237	0	0	0	0
238	0	0	0	0
239	0	0	0	0
240	0	0	0	0
241	0	0	0	0
242	0	0	0	0

Table C-7. (Concluded)

Address	Outputs D0	D1	D2	D3
243	0	0	0	0
244	0	0	0	0
245	0	0	0	0
246	0	0	0	0
247	0	0	0	0
248	0	0	0	0
249	0	0	0	0
250	0	0	0	0
251	0	0	0	0
252	0	0	0	0
253	0	0	0	0
254	0	0	0	0
255	0	0	0	0

APPENDIX D

ANNEX A TO RECOMMENDATION G.703
DEFINITION OF THE HDB3 CODE

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. The HDB3 signal is pseudoternary; the three states are denoted as B+, B-, and 0.

2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces, however, special rules apply (see 4 below).

3. Marks in the binary signal are coded alternately as B+ and B- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (see 4 below).

4. Strings of four spaces in the binary signal are coded according to the following rules:

   a. The first space of a string is coded as a space if the preceding mark of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself; it is coded as a mark (not a violation, i.e., B+ or B-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.

      This rule ensures that successive violations are of alternate polarity so that no dc component is introduced.

   b. The second and third spaces of a string are always coded as spaces.

   c. The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V+ or V- according to their polarity.

GLOSSARY

AMI	Alternate Mark Inversion
BCI	Bit Count Integrity
BITE	Built-in Test Equipment
CEPT	Conference of European Post and Telecommunications Administration
dc	Direct Current
DCC	Digital Communications Corporation
DCEM	Digital Channel Efficiency Model
DCS	Defense Communications System
DEB	Digital European Backbone
DRAMA	Digital Radio and Multiplex Acquisition
ECL	Emitter Coupled Logic
FDM	Frequency Division Multiplex
FIFO	First-in First-out
HDB3	High Density Binary 3
IC	Integrated Circuit
IR	Input Ready
kb/s	Kilobits Per Second
LED	Light Emitting Diode
LOS	Line-of-Sight
LSB	Least Significant Bit
Mb	Megabit
Mb/s	Megabit Per Second
MBS	Mission Bit Stream
MBS A	Mission Bit Stream A
MBS B	Mission Bit Stream B
MHz	Megahertz
ms	milliseconds
NATO	North Atlantic Treaty Organization
NRZ	Nonreturn to Zero
ns	Nanoseconds
PROM	Programmable Read-Only Memory

RADC	Rome Air Development Center
SCBS	Service Channel Bit Stream
SHAPE	Supreme Headquarters Allied Powers Europe
TDM	Time Division Multiplex
TTL	Transistor - Transistor Logic
V	Volts
VCXO	Voltage Controlled Crystal Oscillator
μs	Microsecond